ANALOG + DIGITAL VLSI DESIGN NOTES

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Analog and Digital VLSI Design Notes, First Edition

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More content available at: www.Akshansh.weebly.com

* Module ≡ Counters, say
then leaf cells ≡ Flip flops

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VLSI

INTRODUCTION

→ a representation

☆ Y-CHART (RB1, pg 369-370)

↳ Illustrates a design flow for most logic chips, using design activities on 3 diff domains (that resemble the letter y)

- Behavioral domain
- Structural domain
- Geometrical Layout Design.

fig 14.3

* Y-chart evolution (T1, pg⇒ 9-14)
  * See what kind of chip to make (Design varies)
  * Do floor planning (which component to put where)
  * Develop each block
  * Connect each block
  * Reduce transmission speed delays
  * Boolean algebra simplific" & then making ckt
  * Making the chip from Smithy shop.

* Simplified view of VLSI design flow: (T1, pg 9-14)
  → bidirectional ⇒ when an already prepared chip has to be added/changed with exc custom parameter.
  ↳ So, both top-down & bottom-up approaches are req'd

☆ Challenges in Digital Design

∝ DSM

Microscopic Problems

- Ultra high speed design
- Interconnect
- Noise
- Reliability
- Power Dissipation
- Clock distrib^n.

∝ $\frac{1}{DSM}$

Macroscopic

- Time to market
- Millions of gate to make
- High level abstractions
- Portability
- Predictability

etc

∴ VLSI design

∴ micro & nano tech

☆ CMOS

- nMOS ($V_T \sim 0.7V$)
- PMOS ($V_T \sim -0.7V$)

(if not $= V_{gs} - V_t$)

Dir^n of current

nMOS: Drain, Gate, Body, Source

PMOS: D, G, B, S

or G, D, S

(mainly used as a 3 terminal device)

- Imp. elements :
- Power dissip^n
- Speed ($\propto \frac{1}{delay}$)
- Area of chip
- reliability → only for nano

G, D, S

Channel width

Thickness

Source

W

G

D

T

OXIDE

x_j { n^+ ← L → n^+

I_{ds}

nmos

P substrate

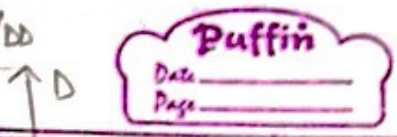
Body

★ The channel length (L) :

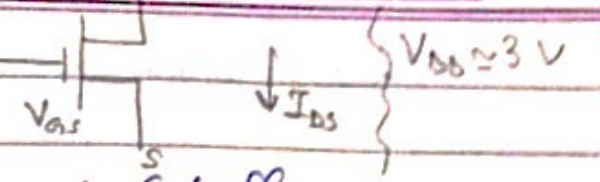
$\simeq 10^{-6}$ m (μm) : Micron tech.

$\simeq 10^{-9}$ m (nm) : Nano technology

Transistor ≡ SWITCH



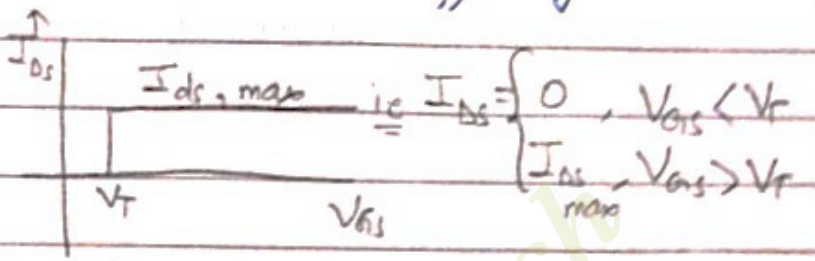
• Common relations:-

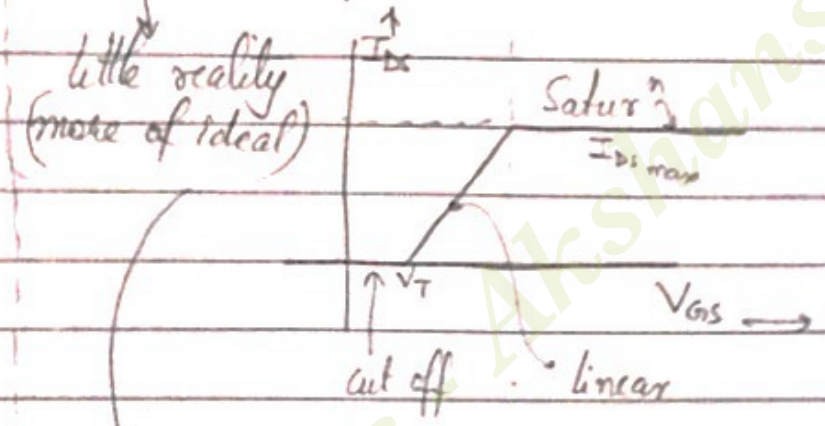


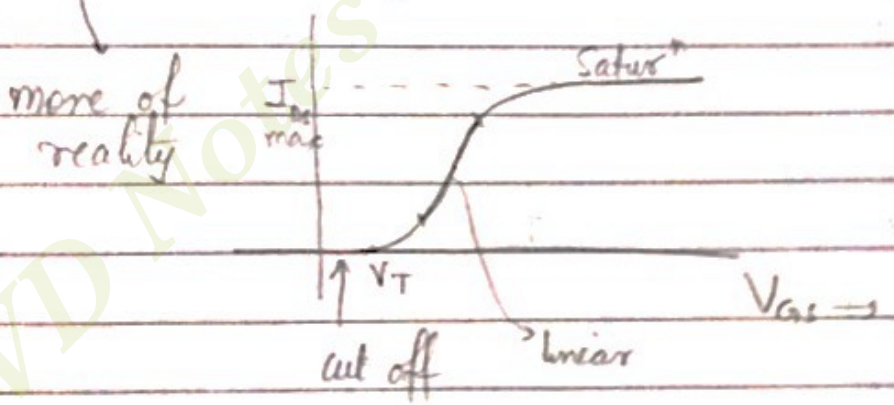
Ideal Behaviour

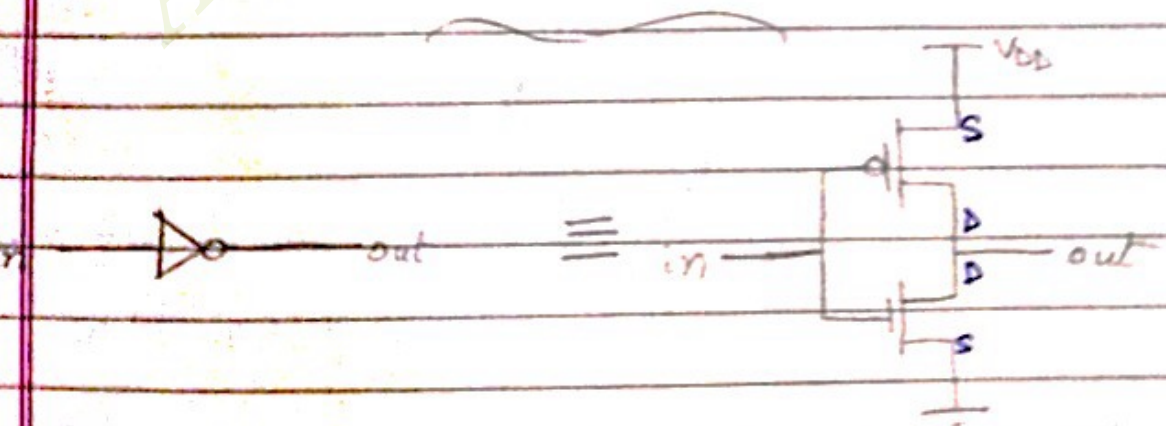
Open ckt

$V_{GS} < V_T$: Cut off region.









* PTM: Predictive Technology Model

(# ptm.asu.edu)

* $\frac{\text{Width}}{\text{length}} = \frac{W}{L}$ = called as ASPECT RATIO

Geometry of transistor

Puffin

* Codes used in modelling

∃ diff levels of models. Codes vary for every level.

Whenever you see — Stands for

MP1 — Pch (PMOS)

Mn1 — nch (NMOS)

l, w — length, width of channel

eg the code statement :-

MP1 VDD in out VDD

Mn1 Vss in out Vss

Vss = Source/Body, in = Gate, out = Drain, VDD = Body/Source

eg (2) V1 vdd 0 3V

way of modelling

VDD = 3V

* Mathematics involved in MOS theory :

- $V_{gs} < V_t$ ⇒ MOSFET in cut off region.

  V_t = threshold voltage ⇒ $I_{ds} = 0$.

  (∀ PMOS & NMOS)

- $V_{gs} > V_t$ & $V_{ds} < V_{gs} - V_t$

  ⇒ MOSFET is in linear region.

  ⇒ $I_{ds} = \frac{\mu \epsilon_{ox} W}{T_{ox} L}\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$

  ϵ_{ox} = Permittivity of oxide layer

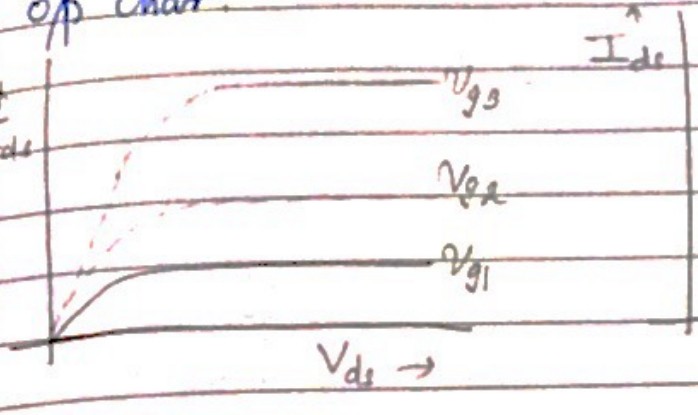
- $V_{gs} > V_t$ & $V_{ds} > V_{gs} - V_t$

  ⇒ MOSFET is in saturation region.

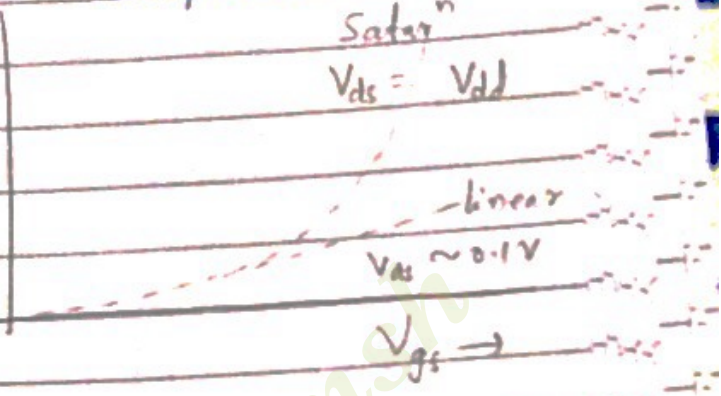
  ⇒ $I_{ds} = \frac{\mu \epsilon_{ox} W}{T_{ox} L}\left(\frac{(V_{gs} - V_t)^2}{2}\right)$

I-V Char. of transistor

o/p char.



Transfer char.



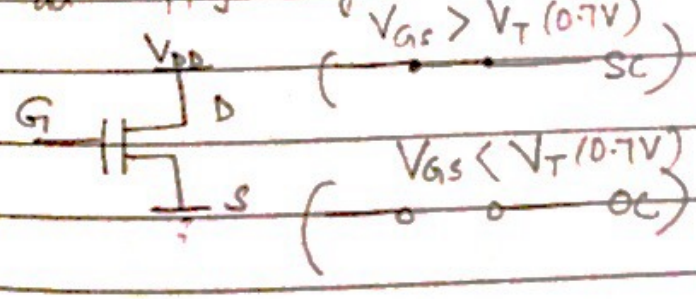
- Note :-
  - I_{ds} is const & independent of V_{ds} in satⁿ.
  - I_{ds} is zero in sub threshold region
    - ∴ $V_{GS} < 0.7V$ ⇒ open switch

→ Identities incorrect → especially for sub micron MOS transistor

✡ Working on I_{ds} formula under Saturation :-

$$I_{ds} = \frac{1}{2} \mu_n \frac{\epsilon_{ox}}{T_{ox}} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2}$$

- N_a, N_d : doping conc.
- V_{dd} : supply voltage



★ CONSTANT FIELD SCALING.

✓ If you change one parameter, what change comes in other parameters :-

- Primary scaling factors

DO THIS

- T_{ox}, L, W, X_j (all linear dimensions) $\rightarrow 1/k$
- N_a, N_d (doping conc.) $\rightarrow k$
- V_{dd} (supply voltage) $\rightarrow 1/k$

- Derived scaling behaviour of transistor

THIS

- Electric field $\rightarrow 1$
- I_{ds} $\rightarrow 1/k$
- Capacitance $\rightarrow 1/k$

HAPPENS

- Derived scaling behaviour of circuit
- Delay ($RC = (\frac{V}{I})C$) $\rightarrow 1/k$
- Power (VI) $\rightarrow 1/k^2$
- Power-delay product $\rightarrow 1/k^3$
- Circuit density ($\propto 1/A$) $\rightarrow k^2$

Verifying, in the I_{ds} formula of saturⁿ,

eg :- If this is done

$V_{DD} \rightarrow \frac{V_{DD}}{k} (V'_{DD})$

$V_{GS} \rightarrow \frac{V_{GS}}{k} (V'_{GS})$

$V_T \rightarrow \frac{V_T}{k} (V'_T)$

$T_{ox} \rightarrow \frac{T_{ox}}{k} (T'_{ox})$

$W \rightarrow \frac{W}{k} (W')$

$L \rightarrow \frac{L}{k} (L')$

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Formula changes as:

$$I_{DS}' = \frac{1}{2}\mu_n\left(\frac{\epsilon_{ox}}{T_{ox}'}\right)\left(\frac{W'}{L'}\right)\frac{(V_{GS}' - V_T')^2}{2}$$

$$= \frac{1}{2}\mu_n \frac{\epsilon_{ox}}{(T_{ox}/k)} \frac{(W/k)}{(L/k)} \frac{(V_{GS}/k - V_T/k)^2}{2}$$

$$= \frac{I_{DS}}{k}$$

$\therefore I_{DS} \rightarrow \frac{I_{DS}}{k}$ (verified).

Ily, $T' = R'C'$

$$= \frac{V_{DS}/k}{I_{DS}/k} \times \frac{C}{k}$$

$$\Rightarrow T' = \frac{T}{k}.$$

Verifying

$$C_{GS} = C_{ox} \times W \times L = \frac{\epsilon_{ox}}{T_{ox}} \times W \times L$$

(Transforming)

$$C_{GS}' = \frac{\epsilon_{ox}}{(T_{ox}/k)}\left(\frac{W}{k}\right)\left(\frac{L}{k}\right) = \left[\frac{\epsilon_{ox}}{T_{ox}} \times W \times L\right]\frac{1}{k} = \frac{C_{GS}}{k}.$$

C_{GS}' → C_{GS} after scaling

* CONSTANT VOLTAGE SCALING:

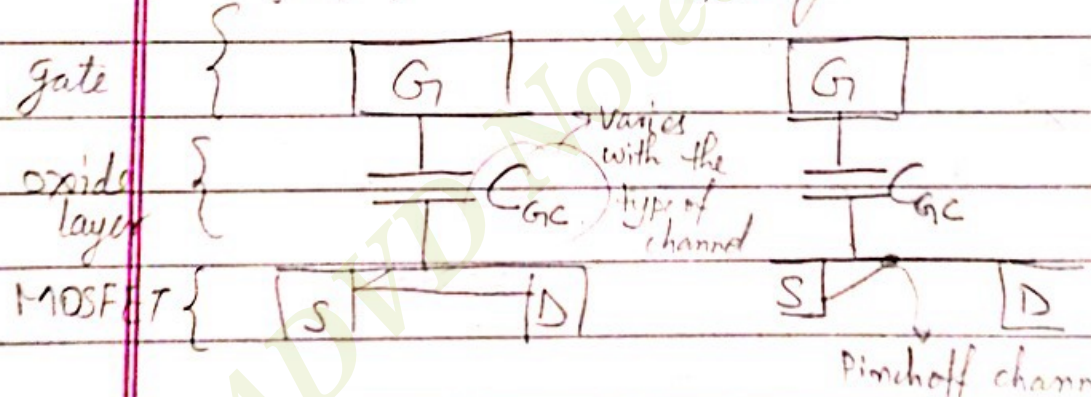
V_{dd} (voltage) = → 1 (constt)
V_{GS}, V_{DS} → No change

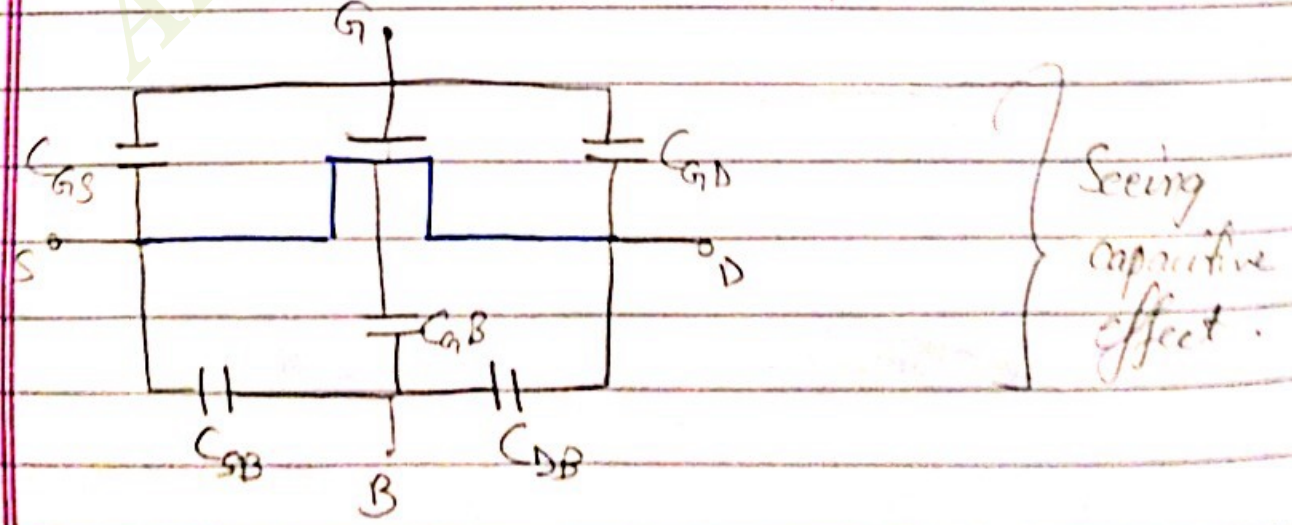
ideally assumption

Capacitance (C_{GS}) → $1/k$
Current (I_{ds}) → k
Delay (τ) → $1/k^2$
Power → k
Power-delay product → $1/k$
Circuit density → k^2

✡ Characteristics of MOS (in graph): Seen practically

Seeing capacitance C_{GC} (gate to channel cap.)





★ $I_{ds} \propto V_{GS}, V_T, V_{DS}$

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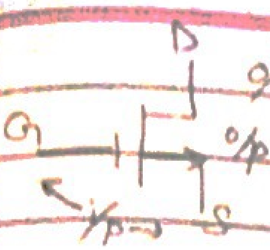


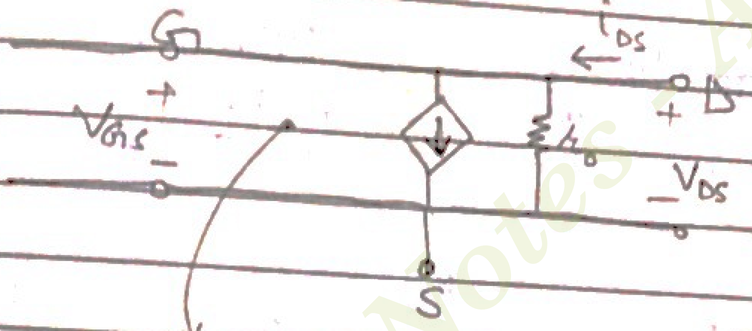
o/p Conductance, $g_o = \left.\dfrac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{GS}, V_{SB} \text{ constt}} = \dfrac{1}{r_o}$ (resistance)

Transconductance, $g_m = \left.\dfrac{\partial I_{ds}}{\partial V_{GS}}\right|_{V_{DS}, V_{SB} \text{ constt}}$

$g_{mb} = \left.-\dfrac{\partial I_{ds}}{\partial V_{SB}}\right|_{V_{GS}, V_{DS} \text{ constt}}$

★ Large Signal Model ≡ Saturⁿ Region

$(V_{DS} \geq V_{GS} - V_T)$



$i_{DS} = \dfrac{\mu \epsilon_{ox}}{T_{ox}} \dfrac{W}{L} (V_{GS} - V_T)^2$

- Typical values for 0.35 μm technology for a situation : 3.3V, $L = 0.35\,\mu m$, $W = 0.7\,\mu m$, $T_{ox} = 7\,nm$, $V_{T0} = 0.6\,V$, $V_{gs} - V_t = 1\,V$

$g_m \sim 10^{-4}\,A/V$ $1/g_m \sim 10\,k\Omega$

$g_{mb} \sim 0.1\,g_m \sim 10^{-5}\,A/V$ $1/g_{mb} \sim 100\,k\Omega$

$g_o \sim 0.01\,g_m \sim 10^{-6}\,A/V$ $1/g_o \sim 1000\,k\Omega$

f : femto = 10^{-15}

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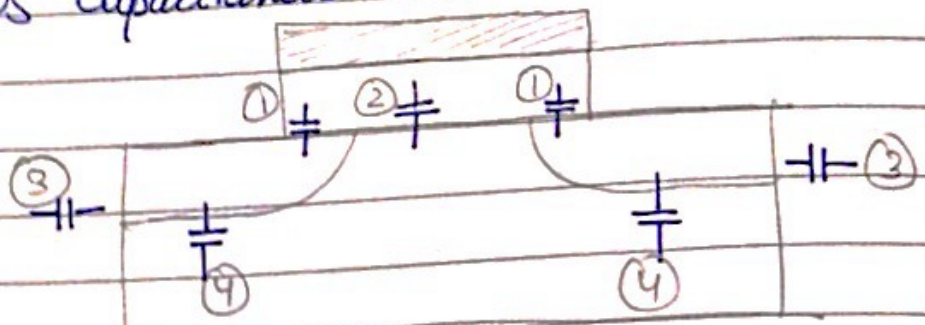
★ MOS Capacitances

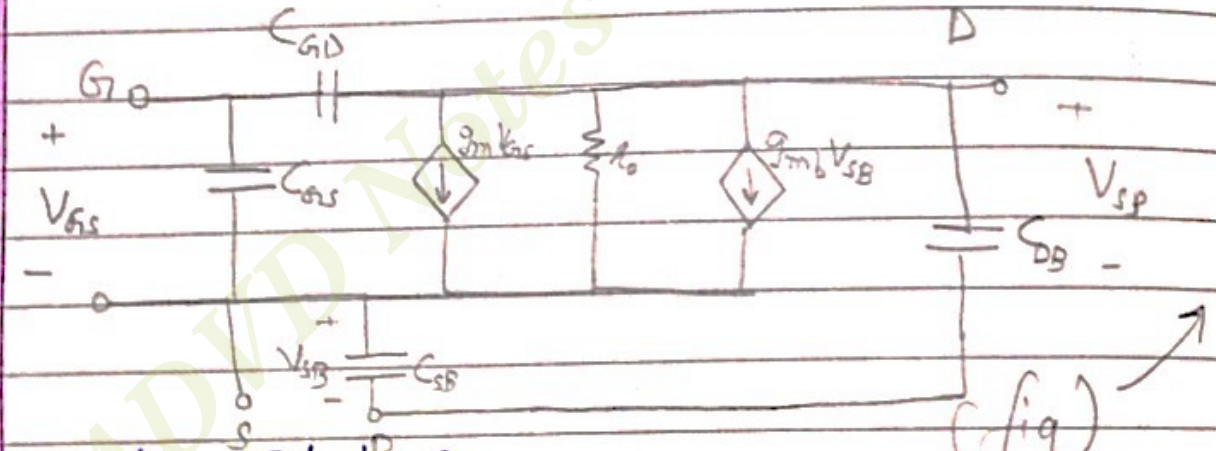


① :- C_{ov} overlap capacitance
gate capacitance that overlaps doped region.
(C_{gdo} / C_{gso})

③ :- C_{jsw} : junction side wall capacitance

④ :- C_j : source/drain bottom plane junction capacitance p.u area

★ MOSFET HIGH FREQUENCY MODEL



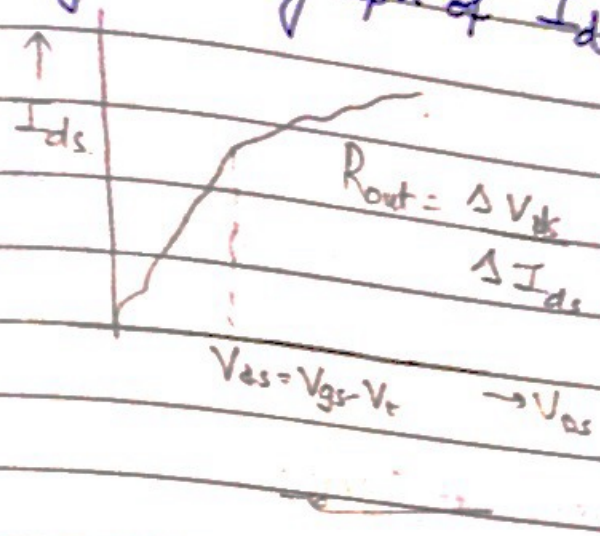
Analysing Non Ideal Cases

(a) ★ Channel Length Modul^n

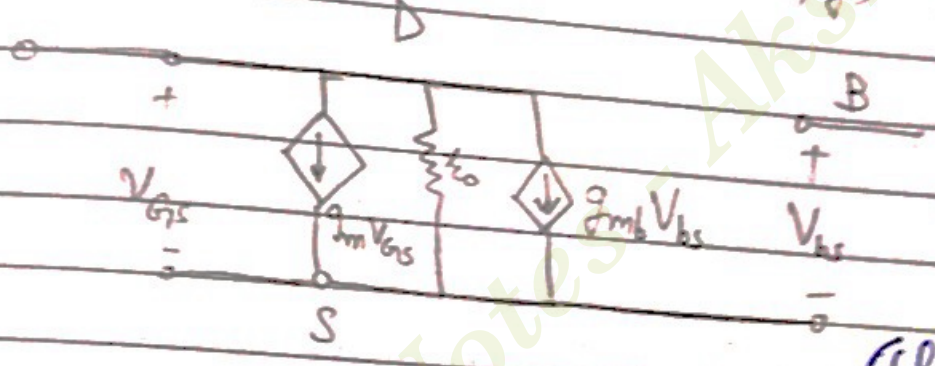
↳ Change in Drain Source current when channel length changes ($L_{eff} = L - \Delta L$) → f(Vds)

$$I_{ds} = \frac{\mu \epsilon_{ox} W (V_{gs} - V_t)^2}{T_{ox} L_{eff} \times 2} \quad \text{or} \quad I_{ds} = \frac{\mu \epsilon_{ox} W}{T_{ox} L} \cdot \frac{(V_{gs} - V_t)^2}{2} (1 + \lambda V_{ds})$$

Changes in graph of I_{ds} vs V_{ds}



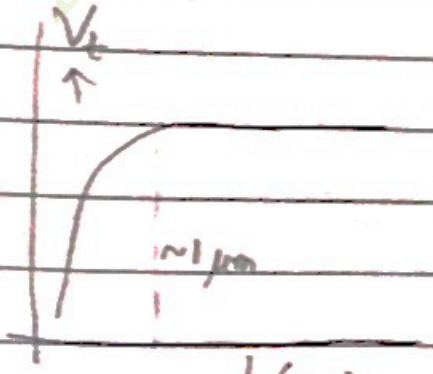
(b) On introducing Body Effect to (fig)



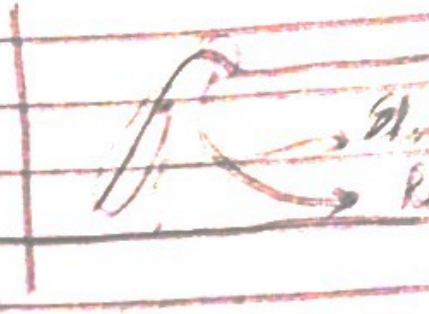
(Change in High frequency model)

(c) Short Channel Effect

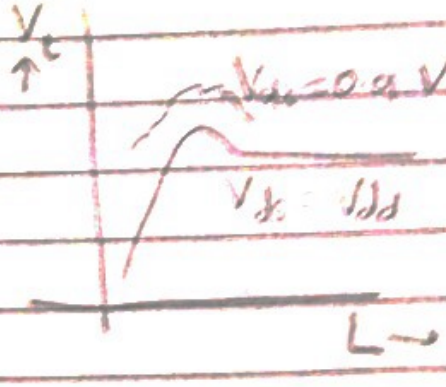
Variations of channel length (L) with V_t



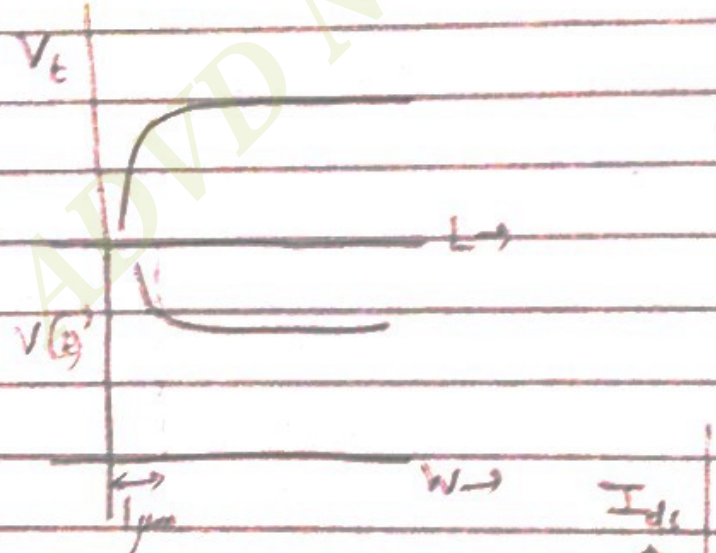
(d) Reverse short channel effect



(e)* Drain Induced Barrier Lowering



(f) Narrow width effect:



(g) Velocity saturation.

↳ $I_{D,sat}$ ↓ :: eff vel. satur^n

(h) Punch through

When 2 depletion overlaps then $V_d > V_{pt}$ (Punch through)

(i) Hot carrier reliability

Typically seen in case of Avalanche breakdown

(j) Gate oxide reliability

Under high electric fields electrons tunnel through the oxide.

Tunneling electrons create damage in the oxide

§ CMOS Design Parameters

T_{ox}, W, L, X_j, V_{DD}, V_T

* **Level 1 Model**

Shichman and Hodges Model

(Ref: T2: Sec 2.4.4 Sec. 16.3.1)

Table 2.1 : Showing values of Capacitances & others

- includes :- eqns for
  - triode / linear region
  - saturn region

* this model does not include sub-threshold conduction or any short channel effects ; maintains reasonable I/V accuracy for channel lengths as small as $\simeq 4\mu m$. Also

* In total, ∃
  16 parameters for NMOS
  & 16 parameters for PMOS
  } Table 2.1 (TB 2)

* Level 2 model
  ↳ The model exhibits moderate accuracy for wide, short transistors.
  V_T : not const.
  ΔL : varies with V_{DS}, $V_{D,sat}$ ....
  μ : C_{ox}, V_{GS}, V_{TH}, V_{DS}.
  γ : introduced.

* Level 3 model :- (Ref TB2, Sec 16.3)
  ↳ (F_n, F_s)
  ↳ Narrow channel ⇒ W is narrow
  ↳ Short channel ⇒ L is short.

* BSIM SERIES (Ref. TB2, Sec 16.3.4)

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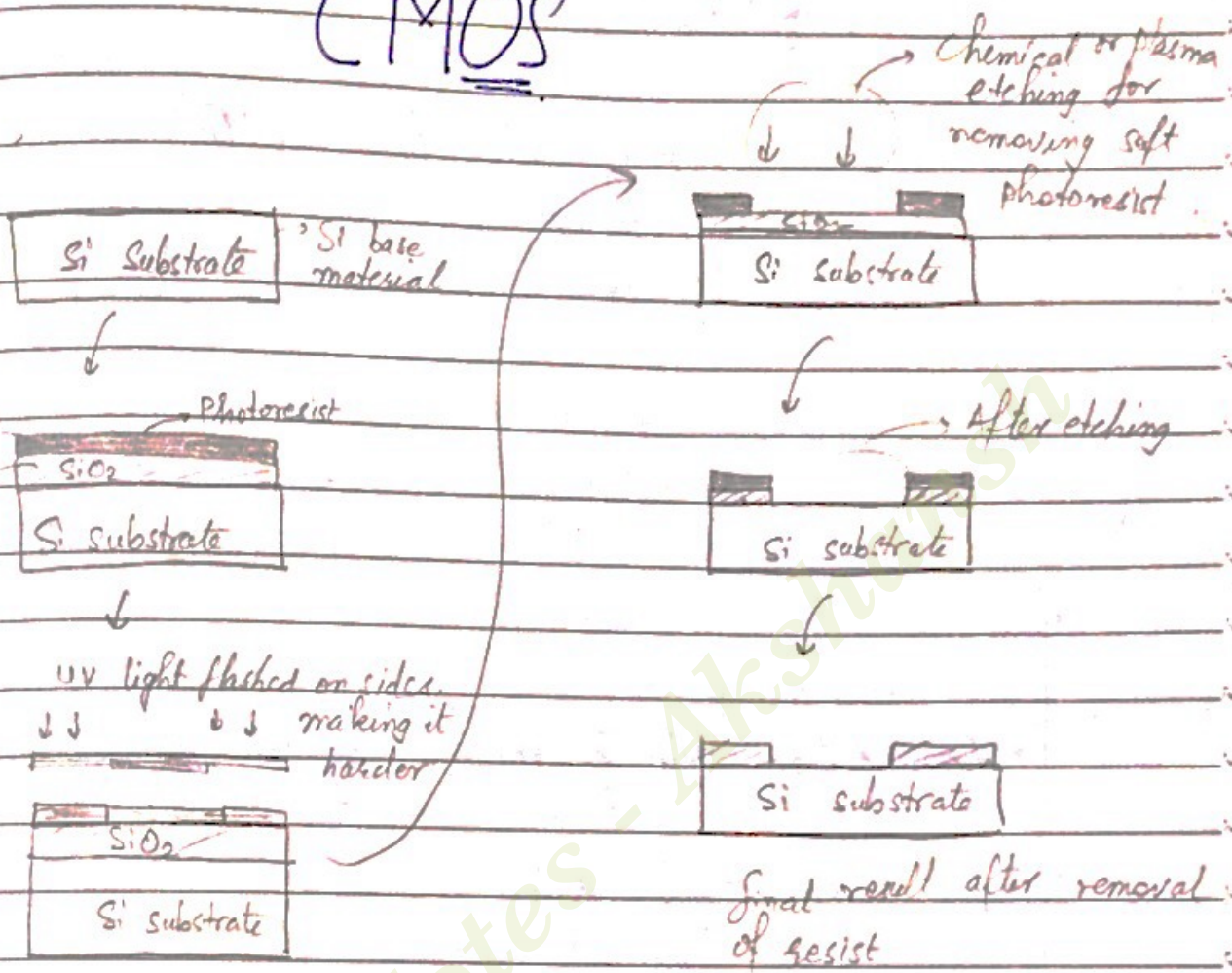
CMOS



comes by deposition

forms an oxide of Si surface

* Gates: made of polysilicon.

* p-well & n-well

In a CMOS, ∃ nmos & pmos together in same structure. But, only one substrate is taken common to both. Now, pmos needs n substrate & Nmos needs p-substrate.

So, if the common substrate is n, then a p-well is created with n mos.

* CMP: Chemical Mechanical Processing

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☆ DESIGN RULES.

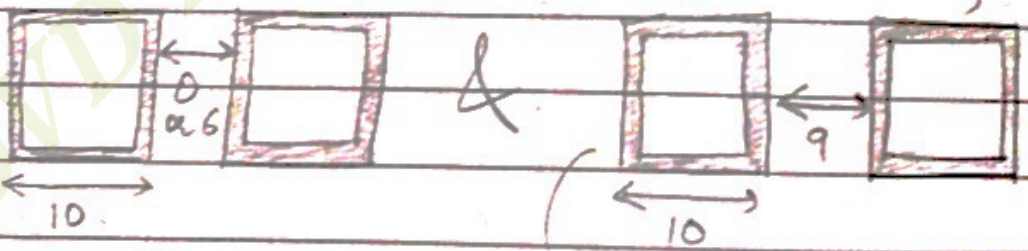
- Unit dimension : min. line width
  - → scalable design rules : λ parameter
  - → absolute dimensions (micron rules)
  - allows design within 0.18 μm – 0.25 μm range (very limited range)

Learn colors

- define we, colours for all layers of a CMOS meant for designing. eg, for well, color is  → yellow
- Connection b/w 2 metal layers, called as "VIA"

- Intra layer design rules: Proportional
  Under what cond^ns & what should be the distance b/w 2 same layers.

eg: Same potential Different potential



⇒ If 2 wells are at same potential, & the width is 10 units, then distance b/w 2 wells is 0 or 6 units.

⇒ If 2 wells are at different potential, distance b/w wells should be 9 units (when width is 10 units)

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* Basically, design of a transistor and other things is seen on the basis of the colors assigned to them
We see bands of diff. colours, connected together making a structure of transistor or any device (view seen is top view or front view)

° Stick diagram:
→ making a ckt. of it, every connection is of different colour to demarkate what connection it is

° Packaging requirements:
→ Electrical: less parasitics
→ Mechanical: reliable and robust
→ Thermal: efficient heat removal
→ economical: cheap

° Bonding: make a circuit design & connect/bond circuit to the base using
Wired bonding
Tape automated bonding
Flip chip bonding
Package-to-board interconnect → Through hole mounting
→ Surface mount

° Package types:
Bare die, DIP, PGA, Small outline, Quad flat pack, PLCC, Leadless carrier
• each type of packaging has some value of C & L (so, speed slows down, resonating effects can come)

* Note: A diode connecting transistor acts as a resistance

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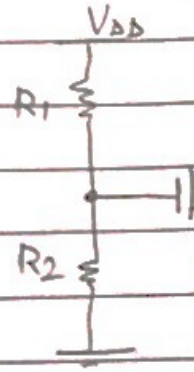
Chapter-5

VLSI IC design

- Current definition by resistive divider

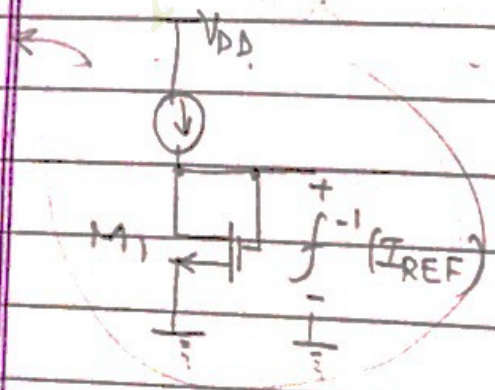


we have nmos → M1.
Assuming it in satur^n ⇒ we have

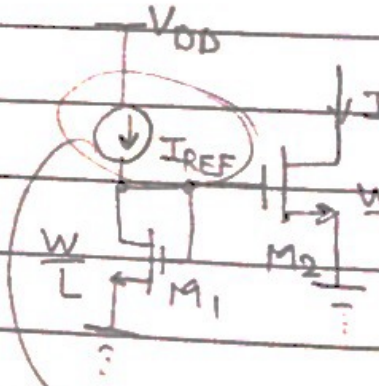
$$I_{out} \simeq \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD}-V_{TH}\right)^2$$

V_{ov} → overdrive voltage

* Idea: for generating an accurate current source, use Reference generator (generating I_{REF})
Now, as Reference generator is costly, so, to use in every circuit, current mirror circuits are used to give I_{REF}
I generate I_{REF}. Now, $I_{REF} = f(V_{GS})$
(I_{REF} is a f^n of V_{GS}).
So, $V_{GS} = f^{-1}(I_{REF})$



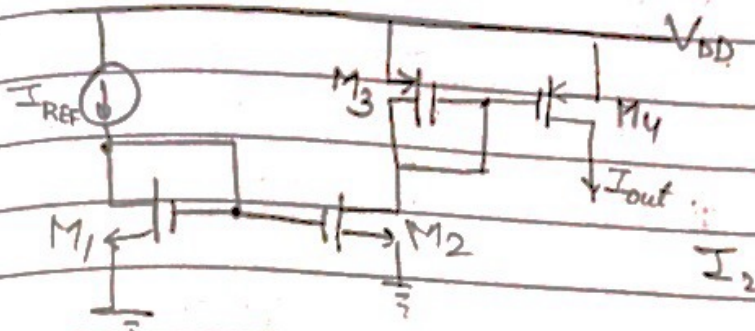
Diode connecting device providing inverse f^n



I_{REF} gets copied.

* CASCODE ≡ CASCADED TRIODES → linear region ≡ Triode region in BJT in FET
↳ combin" of common source & common gate stage.

eg



$$I_2 = I_{REF}\left(\frac{W/L)_2}{(W/L)_1}\right)$$

$$|I_3| = |I_2|$$

$$I_{out} = I_3 \times \frac{(W/L)_4}{(W/L)_3}$$

• In the presence of channel length modulation.

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS}-V_{TH})^2(1+\lambda V_{DS1})$$

& $$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS}-V_{TH})^2(1+\lambda V_{DS2})$$

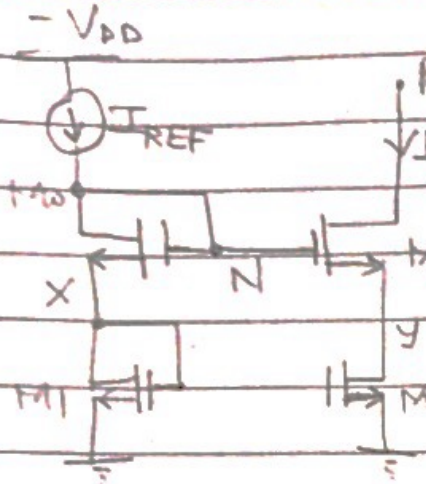
So, $$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1}\cdot\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})}$$ → due to channel length modu"

↳ Ideally, current mirror is :-

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1}$$

* FEATURES OF CASCODE AMPLIFIER (* Basics : Raebey : ch-3,4. Self reading)

- ✓ O/p impedance ↑.
- ✓ intrinsic gain is squared
- ✓ Shielding property
- ✓ i/p pole in presence of Rs is pushed away.



$I_{D2} = I_{D3}$ or I_{out}

$I_{REF} = I_{D1}$

Now

$I_{D2} = \frac{(W/L)_2}{(W/L)_1} \cdot I_{D1}$, or I_{REF}

& $I_{out} = \frac{(W/L)_3}{(W/L)_0} \cdot I_{REF}$

By changing design W & L, we can have

$$\frac{(W/L)_2}{(W/L)_1} = \frac{(W/L)_3}{(W/L)_0}$$

$\Rightarrow I_{D2} = I_{out}$

By this method (see in detail), we can remove channel length modulⁿ.

* ACTIVE CURRENT MIRRORS [Fig. 5.17]

↳ using differential amplifier

↳ use : NOISE CANCELLATION

↳ key parameter : CMRR = A_d/A_c

(Common mode rejection ratio)

tells ⇒ how good my differential amp is?

Some expressions :

- $|A_v| \cong \frac{g_{m1}}{2} [(2r_{o2}) \| r_{o4}]$
- $R_{out} \cong 2 r_{o2}$

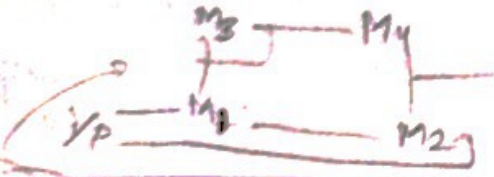


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Fig 5.20 : Symmetric config.

Some imp. parameters useful to see in designing

$R_{out} \simeq (r_{o2} \| r_{o4})$

$A_v \simeq g_{m_{1,2}} (r_{o_{1,2}} \| r_{o_{3,4}}) \Rightarrow g_{m_1} (r_{o_1} \| r_{o_3})$

or $g_{m_2} (r_{o_2} \| r_{o_4})$

$CMRR = \left(1 + 2 g_{m_{1,2}} R_{ss}\right) g_{m_{3,4}} (r_{o_{1,2}} \| r_{o_{3,4}})$

→ common mode rejection ratio.

$$\frac{\Delta V_{out}}{\Delta V_{in,cm}} \cong \frac{(g_{m_1} - g_{m_2}) r_{o3} - g_{m_2}/g_{m_3}}{1 + (g_{m_1} + g_{m_2}) R_{ss}}$$

→ an extra term when $m_1 \neq m_2$

→ assumption, $r_{o3} >> \frac{1}{g_{m_2}}$

* In real life, whenever I have voltage source as i/p ∃ source resistance is also there in it. So, in the presence of R_s, my TF ($\frac{V_{out}}{V_{in}}$) becomes 2nd ord. (wrt denominator), which was 1st order without R_s

* Various parameters whenever anything is designed with transistors (8)

- Input impedance
- O/p impedance
- DC gain
- AC gain
- Power dissipation
- Delay/Speed

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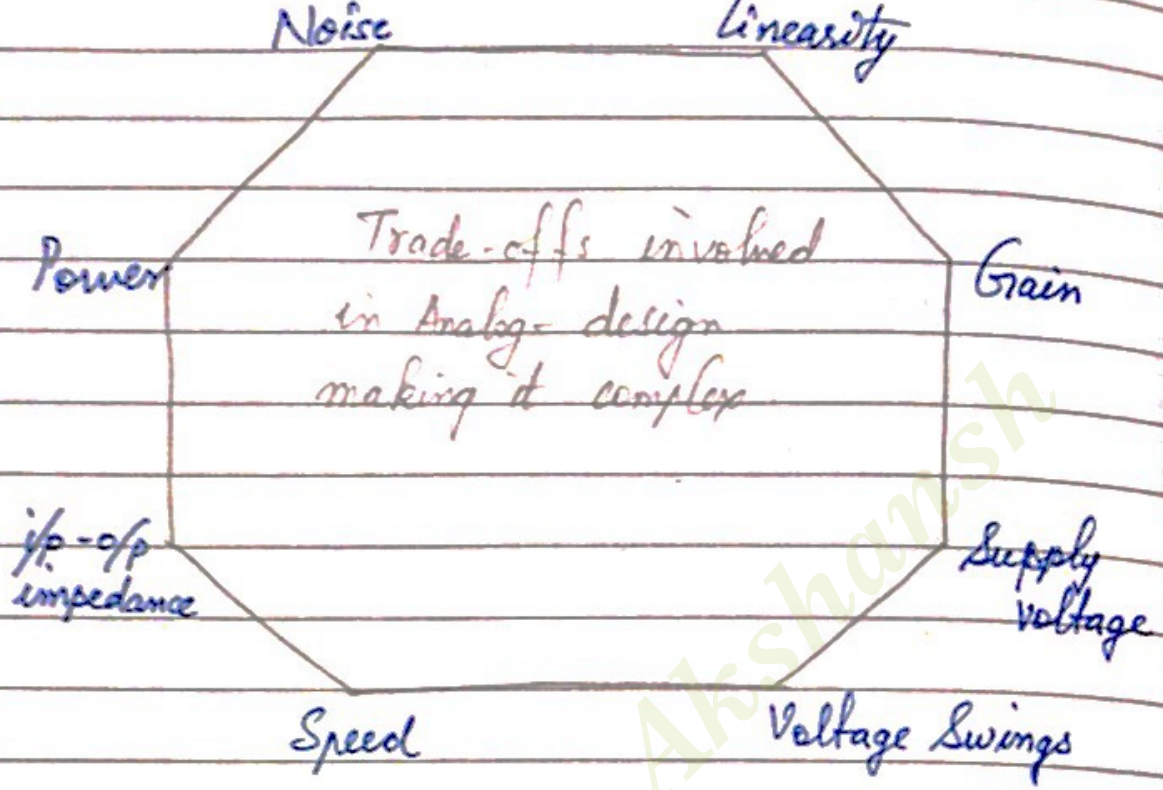
Analog Octagon



(TB : Razavi)

Ch-3

* Source follower config^n (also called Common drain)
  - ↳ seeing high freq response
  - ↳ If pole = zero ∴ Broadband Cond^n.

$$A_v(0) = \frac{C_{gs1}}{C_{gs1} + C_{sb1} + C_{gd2} + C_{db2}}$$

* $\frac{V_{out}}{V_{in}}$ gives high freq char.
* $Z_{out} \simeq \frac{1}{g_m}$; at low freq.
  $\simeq R_s$; at high freq.

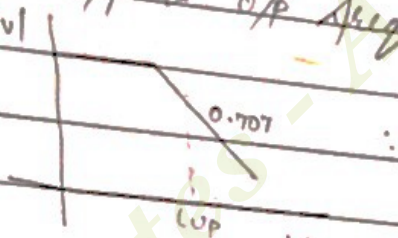
Miller effect ≡ Move a capacitance to some side by multiplying it with some factor

* If impedance ↑ with freq ⇒ Inductive effect

* Similar eqns case seen for Common Gate as well.
  ↳ formulas of $\frac{V_{out}}{V_{in}} \rightarrow Z_L \left(= R_D \left(\frac{1}{C_{DS}}\right)\right)$
  ↳ their analysis

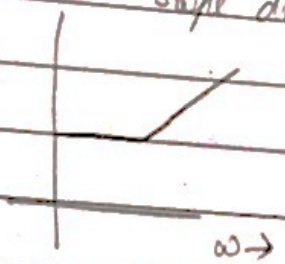
* Concept of poles → Take any 2 nodes, take $\frac{V_{out}}{V_{in}}$ or $\frac{V_{after}}{V_{before}}$ (a Transfer fn. so, has poles & zeros)

In cascode network, ∃ some sort of RC network which restricts the i/p & o/p freq. or anywhere in the graph:



: for one pole.
(for many poles, the slope drops more)

Zeros have the graph like:-



Considering a cascode stage (see fig from book fig 6.25, Razavi)

$$\omega_{P,(A)} = \frac{1}{R_S\left[C_{GS1} + \left(1 + \left(\frac{g_{m1}}{g_{m2} - g_{mb2}}\right) C_{GD1}\right]\right.}$$

point A, at i/p.

i.e., freq. is depending over R & C.

Idea: Go to pt. A & see which R & C components are affecting it

$$\frac{1}{R} \Rightarrow$$

ω_p (x) $= \dfrac{g_{m2} + g_{mb2}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}}$

point X, inside cascode stage

$$\propto \frac{1}{RC}$$

ω_p (y) $= \dfrac{1}{R_D(C_{DB2} + C_L - C_{GD2})}$

point Y, at o/p.

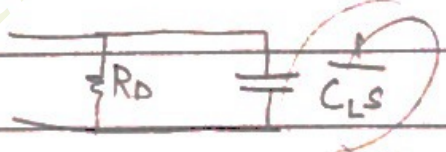
* Learn the idea to analyse the circuit based on the given R's & C's in it.

* Considering Differential amplifier,

At high freq.

$$A_{v,CM} = \frac{(\Delta g_m)\left[R_D \parallel \left(\frac{1}{C_L s}\right)\right]}{(g_{m1} + g_{m2})\left[r_{O3} \parallel \left(\frac{1}{C_{PS}}\right)\right] + 1}$$

At low freq.



→ becomes open circuit at low freq.

$$A_{v,CM} = \frac{(\Delta g_m) \times R_D}{(g_{m1} + g_{m2}) r_{O3} + 1}$$

Fig 6.31

for a Differential amp (with 2 identical NMOS, 2 identical PMOS)

$$A_v = \frac{V_{out}}{V_{in}} = f(g_{mN}, g_{mp}, r_{op}, r_{oN}, C_E, C_L)$$

for such a circuit,

$$\omega_{p1} \simeq \frac{2 g_{mp} (r_{oN} + r_{op})}{(2 r_{oN} + r_{op}) C_E + r_{op}(1 + 2 g_{mp} r_{oN}) C_L}$$

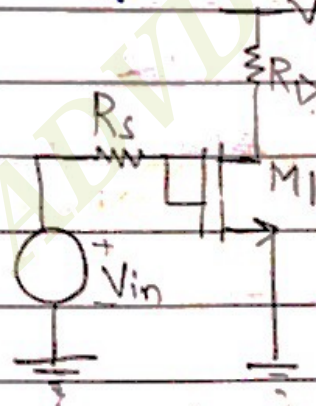
* $$\omega_{p1} \simeq \frac{1}{(r_{oN} \| r_{op}) C_L}$$

→ iff $2 g_{mp} r_{oN} \gg 1$.

→ ω_{p1} depending on NMOS & PMOS resistance & load capacitance.

Assuming: All transistors are in saturation region.

Exercise 6.3



Common source stage.

$R_S = 1 k\Omega$

$I_{D1} = 1 mA$.

$R_D = 2 k\Omega$.

$\frac{W}{L} = \frac{50 \mu m}{0.5 \mu m}$.

Use spice level 1 model to (Table 2.1 Razavi)

→ find poles & zeroes

For poles & zeroes, find voltage gain to make TF.

Now,

$$TF = \frac{V_{out}(s)}{V_{in}} = \frac{(C_{GD} s - g_m) R_D}{(R_S R_D \xi) s^2 + [R_S(1 + g_m R_D) C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})] s + 1}$$

where,

$$\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB}$$

Solving numerator of TF = 0 $\Rightarrow s = \frac{g_m}{C_{GD}} = j\omega$,

or $\omega = \frac{g_m}{C_{GD}}$ (zero)

Solving denominator of TF = 0 (Solving for poles)

$$\omega_{Pole\,1} = \omega_{P_1} = \frac{1}{R_S(1+g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD}+C_{DB})}$$

$$\omega_{P_2} = \frac{R_S(1+g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD}+C_{DB})}{R_S R_D \times \xi}$$

Out of all the above terms, we know R_S, R_D.

Now,

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right) I_D} \quad \rightarrow (1)$$

$$\hookrightarrow \mu_n C_{ox} = (U_0) \times \frac{3.9\,\epsilon_0}{T_{ox}}$$

values taken from Level 1 spice model

$$= 350 \times \frac{3.9 \times 8.854 \times 10^{-14}}{9 \times 10^{-9}}$$

$$= 134.225\ \mu A/V^2$$

$$\Rightarrow g_m = 6.283\ mA/V$$

Now, finding other capacitances,

$$C_{GS} = \frac{2}{3} WL\,C_{ox} + C_{GSO}$$

$C_{GSO} \times W$

$= C_{GDO}$

→ Spice model level 1

* $L_{eff} = 2 - L_D$

$= 0.5\,\mu m - 2(0.08 \times 10^{-6})$

$= 0.34\,\mu m$

(assume $L \to L_{eff}$ ✱ calculations
$W \to W_{eff}$ ✱ calculations
$(W = W_{eff})$

&

$C_{GD} = \frac{2}{3} W L C_{ox} + C_{GDO}$

$C_{GDO} \to C_{GDO} \times W$

$C_{ox} = \frac{3.9 \times 8.85 \times 10^{-14}}{9 \times 10^{-9}}$

$C_{ox} = 0.3835 \times 10^{-6}$

Note
All parameters' value is taken from level 1 spice model table.

After calculations, we find → Junction sidewall capacitance

$C_{GS} = C_{GD} = 20\,fF$

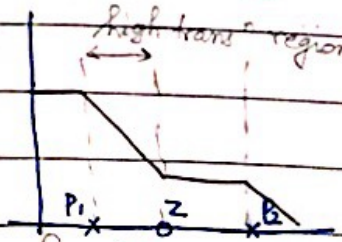
& $C_{DB} = CJ \times AD + CJSW \times PD$

↳ Area of Drain $= W \times L_{eff}$

↳ Perimeter of Drain $= 2\left[\frac{W}{2} + L_{eff}\right]$

↳ Junction capacitance

$C_{DB} = 9.697\,fF$



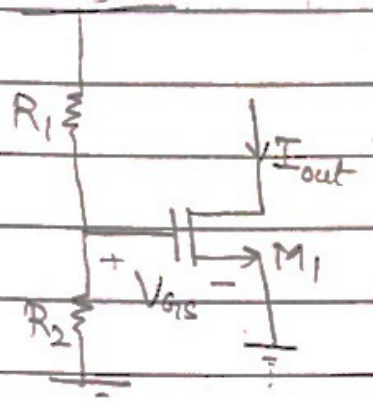
Now finding poles & zeros

Zero $\omega_z = \frac{g_m}{C_{GD}} = \frac{6.283 \times 10^{-3}}{20 \times 10^{-15}}$ & $f = \frac{\omega}{2\pi} \simeq 50\,GHz$

Poles ω_{P_1} or $f_{P_1} = 453.98\,MHz$

ω_{P_2} or corresponding $f_{P_2} = 66.58\,GHz$.

Q 5.1



Given :- $\frac{W}{L} = \frac{50}{0.5}$

$\lambda = 0$

$I_{out} = 0.5\,mA$.

$V_{DD} = 3\,V$

Assume : M1 is in "satur" region.

Use Level 1 SPICE model.

(a) find $\frac{R_2}{R_1}$

We know $I_{ds} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \simeq 0.5mA$

$I_{ds} \rightarrow I_{out}$ (formula for "satur" region)

$\mu_n C_{ox}$ directly, from Level 1 spice model.

$\frac{W}{L}$ = from last problem

$L_{eff} \rightarrow$ 2-LD

Now

$$V_{GS} = \left(\frac{R_2}{R_1+R_2}\right) V_{DD}$$

$$V_{GS} \simeq \left(\frac{1}{\frac{R_1}{R_2}+1}\right) V_{DD}$$

(all unknown values of V_{DD} & V_{GS} : by level 1 Spice model / what is given)

So, $\frac{R_2}{R_1}$ ✓

Seeing impact of V_{DD}

(b) find sensitivity of I_{out} wrt V_{DD}

chain rule

Now, $\frac{\partial I_{out}}{\partial V_{DD}} = \underbrace{\left(\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\right)}_{\text{constt}}\left[2\left(\frac{R_2}{R_1+R_2}\right)V_{DD} - V_{TH}\right] \times \left(\frac{R_2}{R_1+R_2}\right)$

Seeing impact of V_{TH}

(c) Calculate the change in I_{out} for a 50 mV change V_{TH}

Now, value of V_{TH} (from Level 1 spice model) = 0.7 V (Normalised)

given I_{out} = 0.5 mA

So, for changing, take $V_{TH1} = 0.7\,V \pm 50\,mV$

$= 0.75\,V, 0.65\,V$

(d) Let us assume that $\mu_n \propto \left(\frac{1}{T}\right)^{3/2}$ → Temp

V_{TH} = constt

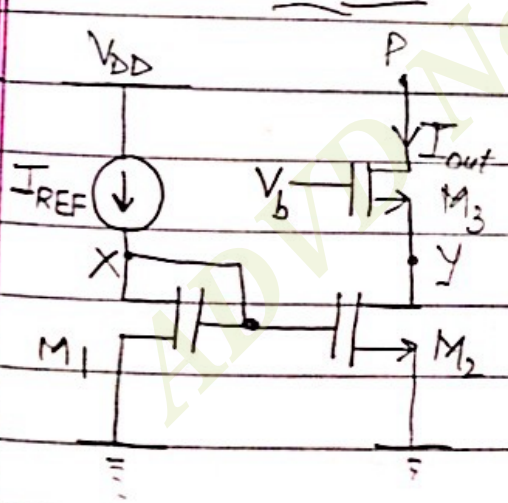
T is increased from 300 K (T_1) to 370 K (T_2)

Now, $I_{DS} \propto \mu_n \Rightarrow \frac{I_{out1}}{I_{out2}} = \frac{\mu_{n1}}{\mu_{n2}} = \left(\frac{T_2}{T_1}\right)^{3/2}$

(I_{out})

(∴, from I_{out} formula, rest all is constt)

Q.5.5



(a) Find V_b for $V_x = V_y$.

Note, $\frac{W}{L}$ is same ∀ FET's.

Now, $I_{ds} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2$ ← constant

Given: $\left(\frac{W}{L}\right)_{1-3} = \frac{40}{0.5}$

(assuming saturn, if nothing given)

$I_{REF} = 0.3\,mA$

$\lambda = 0$ (no channel length modul^n)

from current mirror,

$V_{GS1} = V_{GS2}$

$\Rightarrow I_{ds1} = I_{ds2}$

$V_y = V_b - V_{GS3}$

Now $V_x = V_y$

$\Rightarrow V_x = V_b - V_{GS3}$

$\Rightarrow V_b = V_x + V_{GS3}$

If $V_x \neq V_y$ i.e $V_{DS1} \neq V_{DS2}$

$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2 (1+\lambda V_{DS2})}{(W/L)_1 (1+\lambda V_{DS1})}$

If $V_x = V_y$

$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$

$V_x = V_{GS1}$ (current mirror)

$\Rightarrow V_b = V_{GS1} + V_{GS3}$

Now, from I_{ds} eq", V_{GS} can be found.

$I_{DS1} = I_{REF}$. So, V_{GS1} ✓

Now, $V_x = V_y = V_{GS1}$ ($= V_{GS3, now}$)

So, $I_{DS1} = I_{DS2} = I_{DS3}$ (by the way circuit is connected)

$= I_{out} = I_{REF}$

So, $V_b = V_{GS1} + V_{GS1}$

$\Rightarrow V_b = 2V_{GS1}$ ✓

(b) If V_b changes by 100 mV, how much does I_{REF} & I_{out} differ?

So,

$V_{b,new} = V_b + 100\,mV$

Now, (V_{GS3} → calculated before)

$V_{b,new} - V_{GS3} = V_{y,new}$

So, $V_{y,new}$ ✓

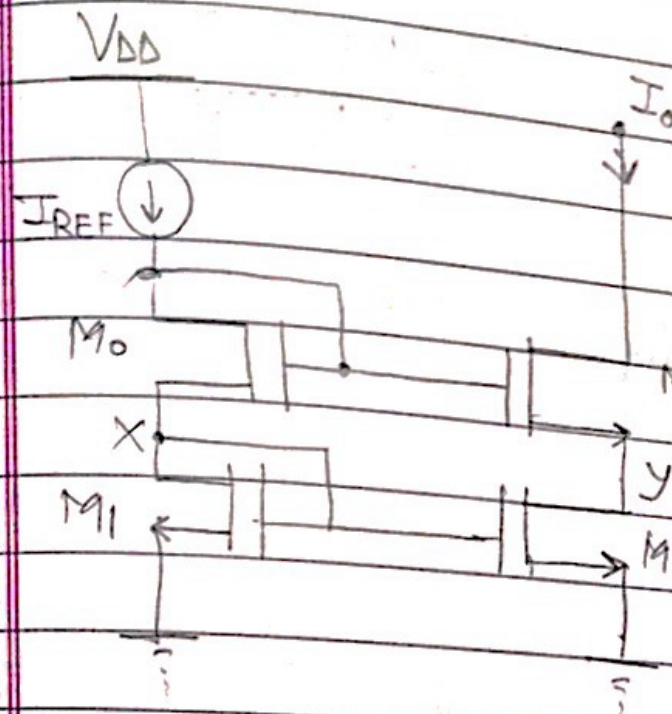
No, we are changing V_b, so, $\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2 (1+\lambda V_{DS2})}{(W/L)_1 (1+\lambda V_{DS1})}$

↳ use this (∵ we changed V_b)

With formula for I_{DS} ($= I_{out}$), we get

$I_{out,new} = (\quad)(V_{GS3,new} - V_{TH})^2$ ✓

(c) Full length cascode current mirror



If V_p changes by 1 V, how much does V_y change?

formula by approxim^n :

$$\Delta V_y \cong \frac{\Delta V_p}{(g_{m3} + g_{mb3}) r_{o3}}$$

Now, $\Delta V_p = 1$

$$g_{mb3} = \gamma g_{m3}$$

$$\Rightarrow g_{mb3} = GAMMA \times \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D}$$

$I_{REF} = 0.3\,mA$

GAMMA → level 1 spice.

$$r_{o3} = \frac{V_{DS3}}{I_{out}}$$

$$r_{o3} = \frac{V_p - V_y}{I_{out}} \rightarrow ?$$

Now, $I_{DS3} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS3})$

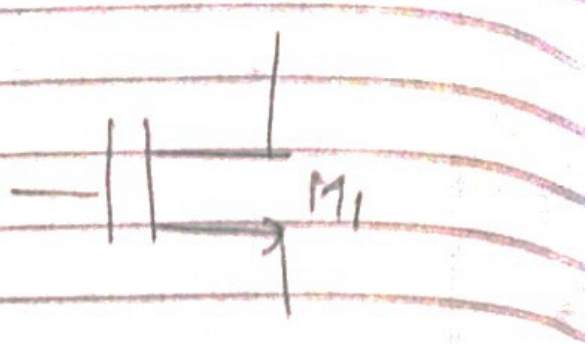
extra term included ∵ V_p was changed

Seeing change in V_y

$$\Delta V_y \cong \frac{\Delta V_p}{g_{m3} r_{o3}} \quad ; \quad \frac{\partial I_{DS3}}{\partial V_{DS3}} = \frac{1}{r_{o3}}$$

Puffin

5. (Parameter change) : Quiz questions



Given $I_{DS} = 100\mu A$

(a) If W changes by 25% what happens to I_{DS}

Note:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

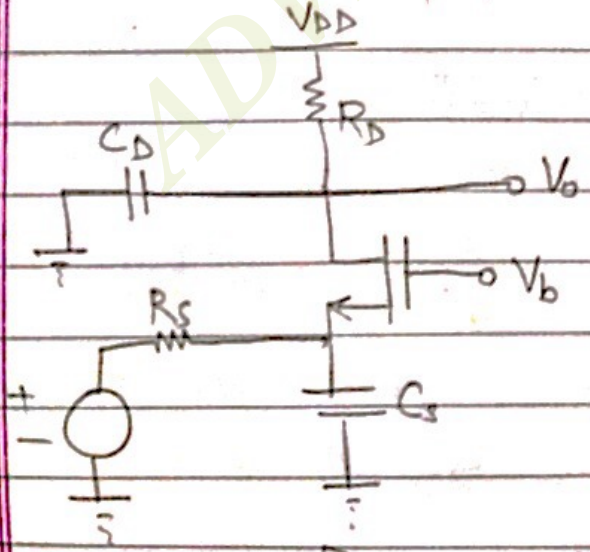
$W \longrightarrow 25\%$

$\therefore I_{DS} \longrightarrow 25\%$ (same) (Directly proportional)

(b) If $V_{GS} - V_{TH}$ changed from 4.3 to 2.3, how does I_{DS} change?

I_{DS} decreases (directly proportional)

6. Common Gate Amplifier



Given :-

$R_D = 2\,k\Omega$

$R_S = 1\,k\Omega$

$g_m = 130.95$.

$g_{mb} = 51.7625$

$C_S = C_D = 14.161\,fF$

$$A_v = \frac{V_{out}}{V_{in}} = \underbrace{\left[\frac{(g_m + g_{mb})R_D}{1 + (g_m + g_{mb})R_S}\right]}_{\text{DC Gain}} \frac{1}{\left(1 + \frac{C_S}{g_m + g_{mb} + R_S^{-1}}s\right)(1 + R_D C_S s)}$$

Or $\frac{V_{out}}{V_{in}} = (\text{DC gain}) * (1 + a_1 s)(1 + a_2 s)$

$\rightarrow a_1 = \frac{C_s}{g_m + g_{mb} + R_s^{-1}}$, $a_2 = R_D C_D$

Now, $(1 + a_1 s)(1 + a_2 s)$

$= 1 + a_1 a_2 s^2 + (a_1 + a_2)s$

$= 1 + a_1 a_2 (j\omega)^2 + (a_1 + a_2)(j\omega)$

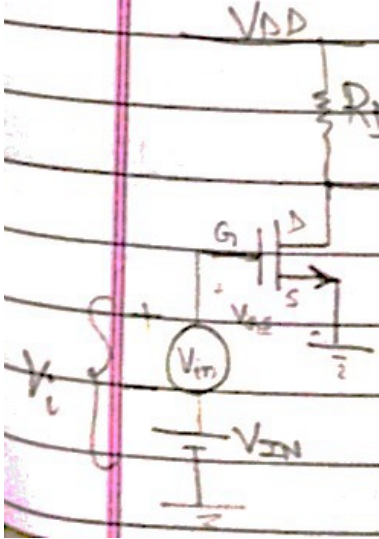
$= (1 - a_1 a_2 \omega^2) + j(a_1 + a_2)\omega$.

$\Rightarrow |A_v| = \frac{\text{DC gain}}{\sqrt{(1 - a_1 a_2 \omega^2)^2 + [(a_1 + a_2)\omega]^2}}$

Q Common source amplifier : formula & analysis

$A_v(s) = \frac{g_m + s V_{GS}}{\underbrace{R_s(C_{GS}C_L + C_{GS}C_D + C_{GD}C_L)}_{a_1} s^2 + \underbrace{(g_m R_s R_D + C_L C_{GS})}_{a_2} s + g_m}$

$|A_v| = \frac{\sqrt{(g_m)^2 + (V_{GS}^2 \omega^2)}}{\sqrt{(g_m - \omega^2 a_1)^2 + \omega^2 a_2^2}}$



① * V_{in} = ~~hf~~ , on this side, FET is in cut off.
To prevent that, add V_{IN}.

~ no past in -ve region

② * If : $R_D \uparrow \Rightarrow$ Gain ↑
(i) But $\Rightarrow$ Power dissip^n ↑ $I_{DS}^2 R_D$
$\rightarrow V_o \downarrow$ (o/p voltage swing is less)
or V_{DS}

So, as $V_o \downarrow \Rightarrow V_o (= V_{DS} = V_{GS} - V_T) \downarrow$

$\Rightarrow V_{DS} < V_i - V_T$. So, transistor goes in linear region

We cannot reduce R_D too much (% Gain ↓)

Now, $V_o = V_{DD} - I_{DS} R_D$

(ii) If: we ↓ I_{DS} ⇒ V_o increases

⇒ o/p voltage swing

now, on decreasing I_{DS}, $V_{GS} - V_T \downarrow$

$\left(\because I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2\right)$

$V_{GS} = V_i$ So, if $I_{DS} \downarrow$, $V_{GS} = V_i \downarrow$.

So, i/p voltage swing ↓ ($V_i - V_T \downarrow$)

Idea:- I/p should accept prev. stage & o/p should drive next stage.

(iii) * If we do $V_{GS} - V_T \downarrow$ & $\left(\frac{W}{L}\right) \uparrow$

⇓ we can make I_{DS} = const^{n}.

Assuming no channel length modul^{n} & satur^{n} region ⇒ size of chip increases.

Now,

$g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)$

Illy as I_{DS}, we keep g_m APPROXIMATELY const^{n}

$\left\{\because I_{DS}$ has $(V_{GS} - V_T)^2 \propto \left(\frac{W}{L}\right)^1$

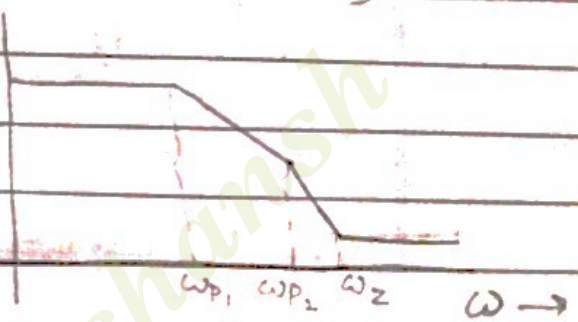
& g_m has $(V_{GS} - V_T)^1 \propto \frac{W}{L}\right\}$

Now, After taking act. values to get cond^n $|\omega_{p_1}| \leq |\omega_{p_2}|$

$$\omega_{p_1} = \frac{}{R_s(1+g_m R_D)C_{GD} + R_s C_{GS} + R_D(C_{GD}+C_{DB})}$$

$$\omega_{p_2} = \frac{R_s(1+g_m R_D)C_{GD} + R_s C_{GS} + R_D(C_{GD}+C_{DB})}{R_s R_D(C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB})}$$

$$\omega_z = \frac{g_m}{C_{GD}}$$



→ If R_s, R_D ↑, ⇒ ω_{p_1} and/or ω_{p_2} ↓,
⇒ BW is reducing

We know,

A_v gain $= -g_m R_D (A_v(s=0))$

$g_m = f(V_{GS} - V_T)$ ⇒ Non linearity

Now,

$$Z_{in} \simeq \frac{1}{[C_{GS} + (1+g_m R_D)C_{GD}]s}$$

If ω/f ↑ ⇒ Z_{in} ↓

By max power transfer theorem
⇒ Power transferred from prev stage goes down.

$$\& \; Z_{out} = \left[\frac{Z_x \times \left(\frac{1}{C_{GS} \times s}\right)}{Z_x + \frac{1}{(C_{GS} \times s)}}\right] \left[Z_x \parallel \frac{1}{sC_{GS}}\right]$$

$$\rightarrow Z_x = \frac{1 + R_D(C_{GD}+C_{DB})s}{sC_{GD}(1 + g_m R_D + R_D C_{DB} s)}$$

Q) Common gate amplifier

$$\text{DC gain} = \frac{(g_m + g_{mb}) R_D}{1 + (g_m + g_{mb}) R_s}$$

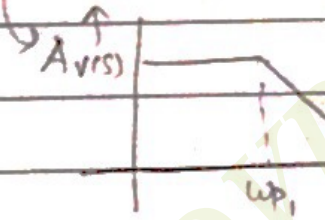
i/p impedance, $Z_{in} \cong \frac{R_D \| \frac{1}{sC_D}}{(g_m + g_{mb}) r_o} + \frac{1}{g_m + g_{mb}}$

↳ $\omega \uparrow \Rightarrow Z_{in}$.

Q) Source follower :

DC Gain $\cong 1$.

$$\omega_{P1} = \frac{1}{R_s C_{GD} + \frac{C_L + C_{GS}}{g_m}}$$



If $R_s = 0 \Rightarrow \omega_{P1} = \frac{g_m}{C_L + C_{GS}}$

$$Z_{in} \cong \frac{1}{sC_{GS}}\left(1 + \frac{g_m}{g_{mb}}\right) + \frac{1}{g_m}$$

↳ for low freq, $g_{mb} \gg |sC_L|$

↳ for high freq, $g_{mb} \ll |sC_L|$

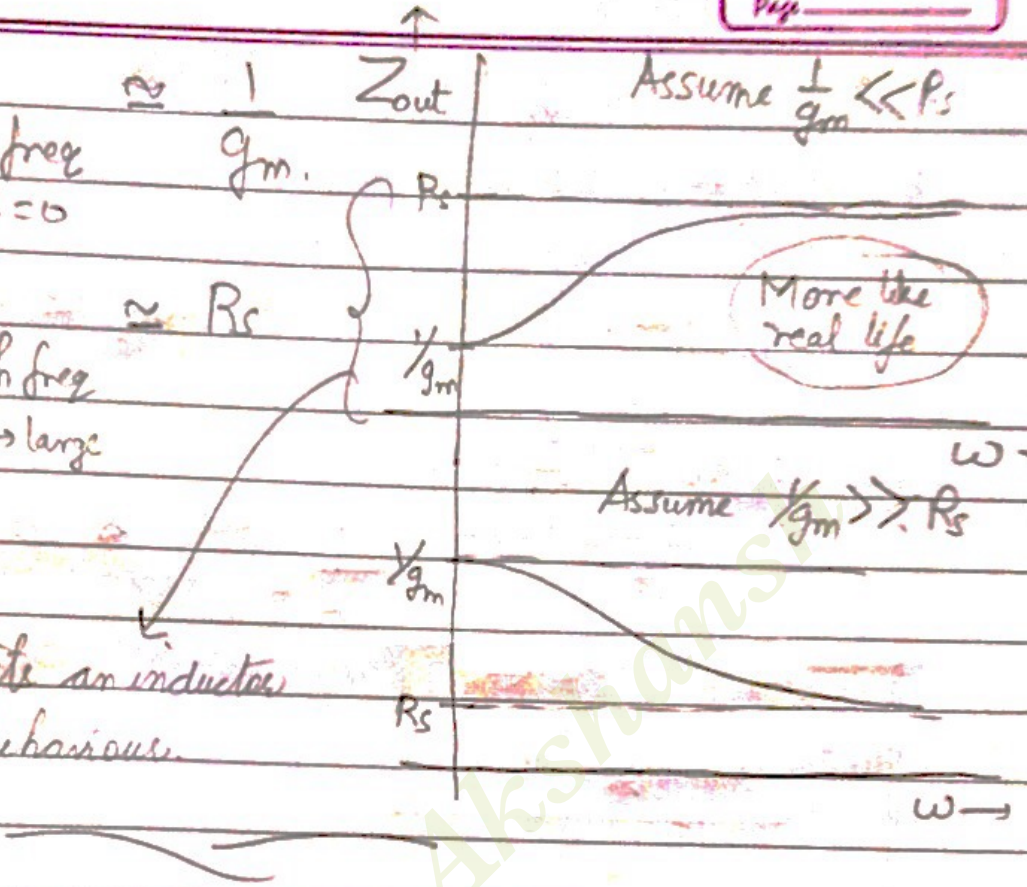
$$Z_{in} \cong \frac{1}{sC_{GS}} + \frac{1}{sC_L} + \frac{g_m}{s^2 C_L C_{GS}}$$

$$Z_{out} = \frac{R_s C_{GS}(s) + 1}{g_m + sC_{GS}}$$

Puffin
Date
Page

Z_{out} | low freq $\Rightarrow s=0$ $\simeq \frac{1}{g_m}$.

Z_{out} | high freq $\Rightarrow s \to$ large $\simeq R_s$



its an inductor behaviour.

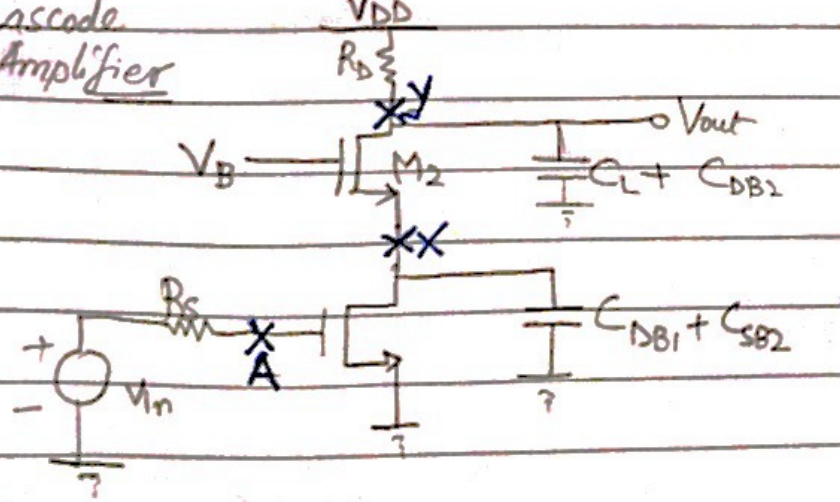
Q. Cascode

$$\omega_{P,A} = \frac{1}{R_s\left[C_{GS1} + \left(1 + \frac{g_{m1}}{g_{m2}+g_{mb2}}\right)C_{GD1}\right]}$$

$$\omega_{P,X} = \frac{g_{m2}+g_{mb2}}{2C_{GD1} + C_{DB1} + C_{SB2} + C_{GS2}}$$

$$\omega_{P,Y} = \frac{1}{R_D\left(C_{DB2} + C_L + C_{GD2}\right)}$$

Cascode Amplifier

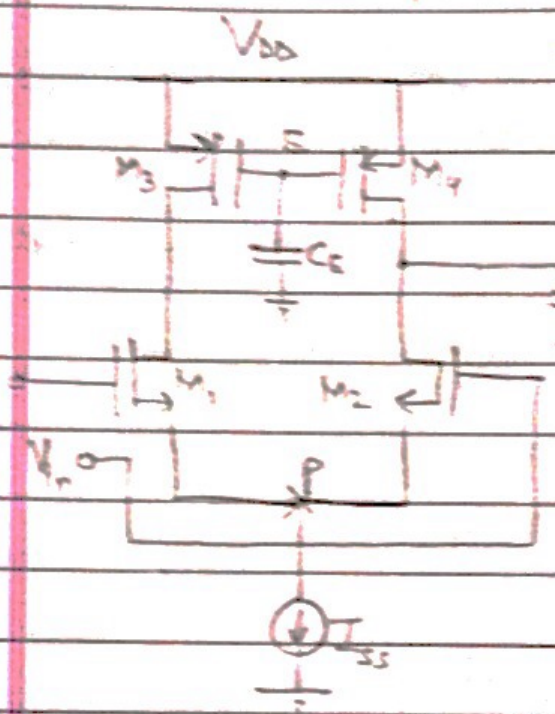


$$Z_{out} = \left(1 + g_{m2}r_{o2}\right)\left(r_{o1} \parallel \frac{1}{sC_X}\right) + r_{o2}$$

Q. Differential Amplifier:

↳ Differential pair:

N: nmos , D: pmos



$$\omega_{D1} \simeq \frac{2g_{mp}(r_{oN} \| r_{oP})}{\left[(2r_{oN} \| r_{oP})C_E + [r_{oP}(1+2g_{mp}r_{oN})C_L\right]}$$

* If $2g_{mp}r_{oN} >> 1$

$$\omega_{p_1} \simeq \frac{1}{(r_{oN} \| r_{op})C_L}$$

(by seeing only RHS of circuit)

$$\omega_{p2} = \frac{g_{mp}}{C_E}$$

Replacing M_3 & M_4 with R_D

$$\Rightarrow A_{V,CM} = \frac{\Delta g_m [R_D \| (1/sC_L)]}{(g_{m1}+g_{m2})[r_{o3} \| \frac{1}{sC_p}] + 1}$$

Common mode

Chapter - 7

NOISE

$$P_{av} = \frac{1}{T}\int_{-T/2}^{T/2} \frac{v^2(t)}{R_L}\,dt$$

↓

Avg. power (= Avg. heat dissipated in the resistance, R_L)

* $v(t)$ is periodic with period T.

* For a random signal,

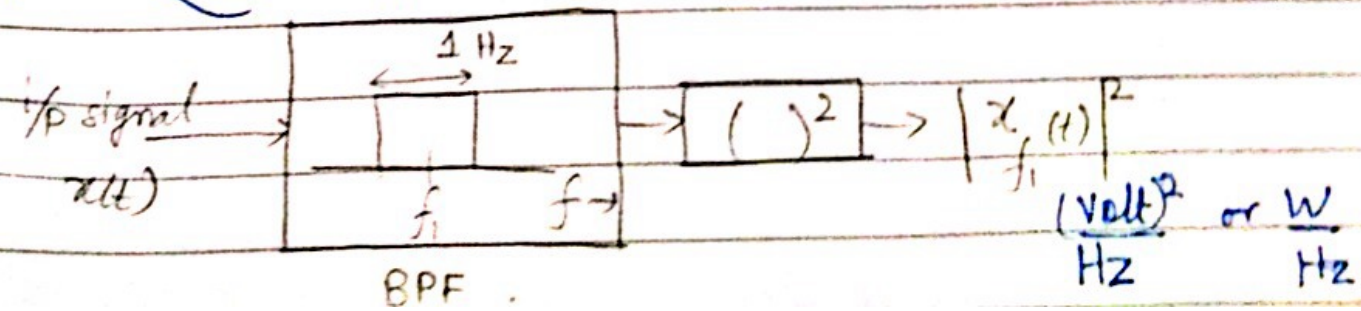
$$P_{av} = \lim_{T\to\infty}\int_{-T/2}^{T/2} \frac{x^2(t)}{R_L}\,dt \quad \text{Watts.}$$

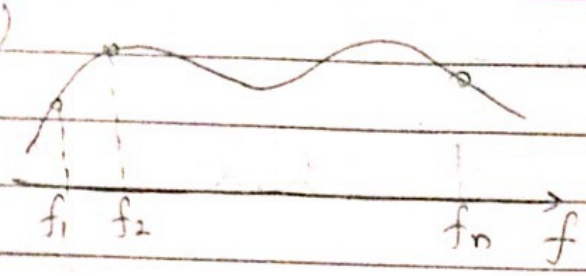
↳ Generally, R_L limit is not taken, so,

$$P_{av} = \lim_{T\to\infty}\int_{-T/2}^{T/2} x^2(t)\,dt \quad \text{Volt}^2$$

* RMS voltage for noise = $\sqrt{P_{av}}$

* Noise Spectrum





Now, $S_x(f)$ (PSD) $= \frac{V}{\sqrt{Hz}}$

(Power Spectral Density)

Q Given:- we have

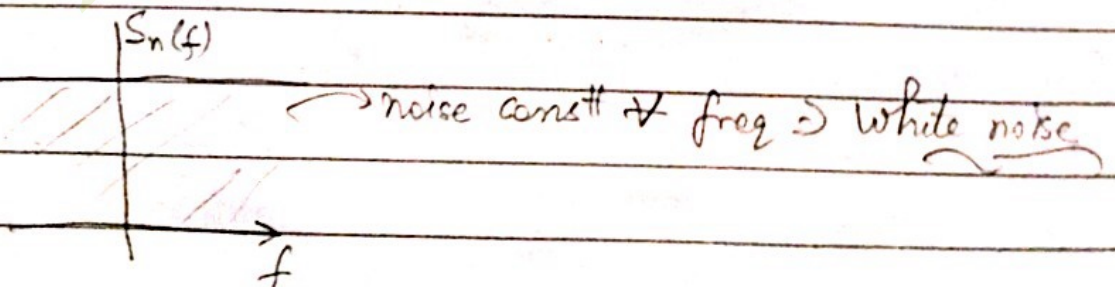
$\frac{3\,nV}{\sqrt{Hz}}$ at 100 MHz $\rightarrow f_1$

$\hookrightarrow$ = Avg. power in 1 Hz BW at 100 MHz

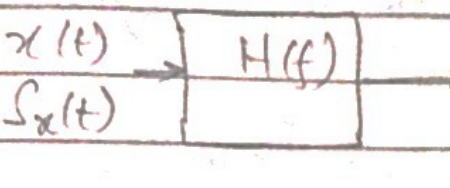
By squaring the term, for power

So, $\left(\frac{3\,nV}{\sqrt{Hz}}\right)^2$ at 100 MHz.

$= (3 \times 10^{-9})^2 \frac{V^2}{Hz}$ at 100 MHz



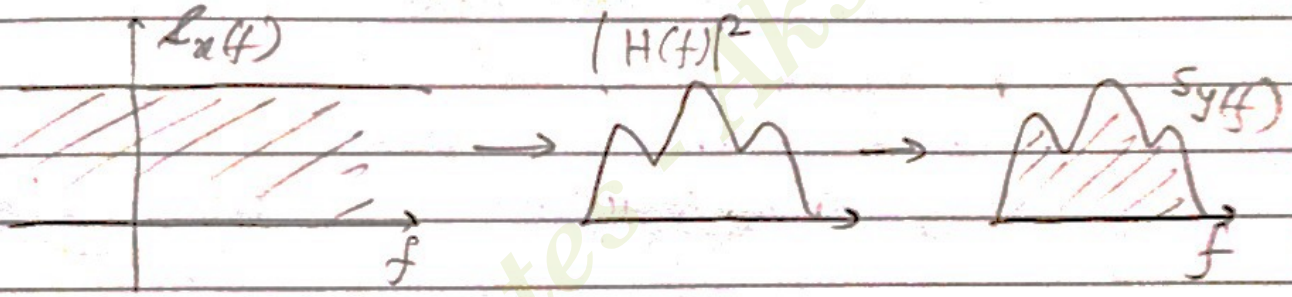
Now,



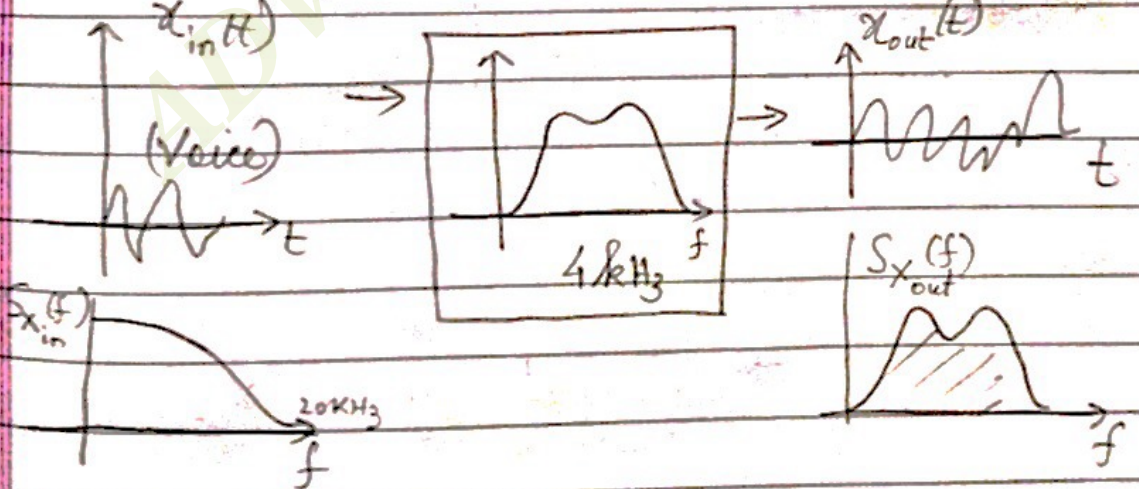
$H(f) = H(s = 2\pi jf)$

$$S_y(f) = |H(f)|^2 S_x(f)$$ → Relation b/w o/p & i/p spectral density (a theorem).

Idea

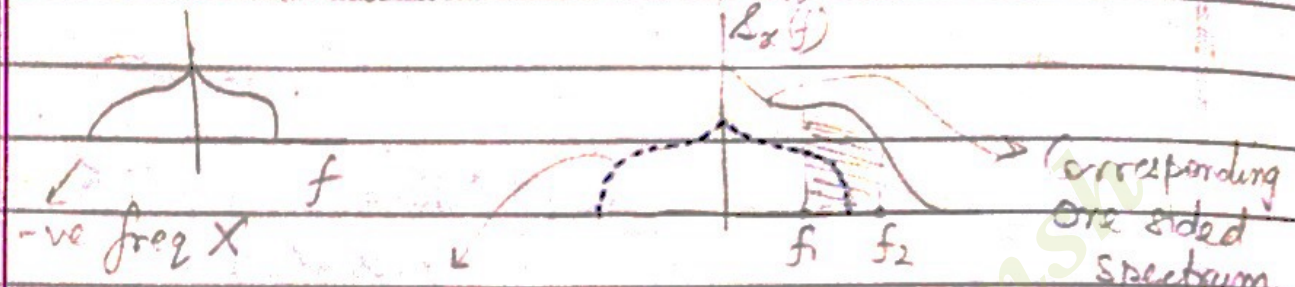


Ex) Considering a telecom sys:



☆ Two sided vs One sided spectrum.

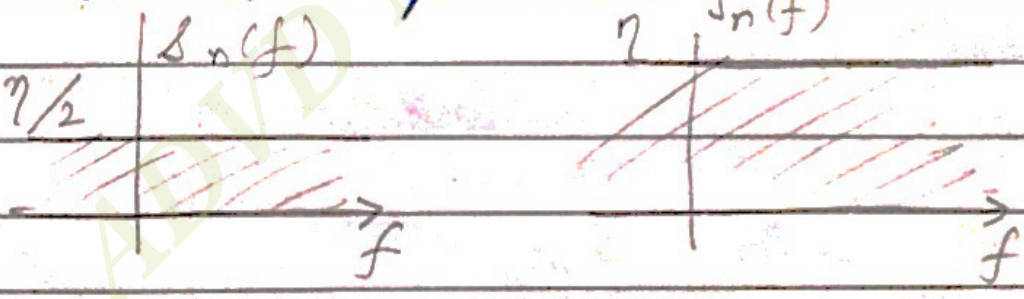
→ Non realistic → Realistic



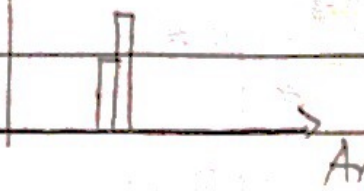
Powers remains same (∵ area for -ve or +ve freq. remains same)

$$P_{f_1,f_2} = \int_{f_1}^{f_2} 2 S_x(f)\,df$$

• Folded White Spectrum



$n(t)$: histogram.



• Correlated / uncorrelated random processes

Consider 2 random signals $x_1(t)$ & $x_2(t)$ (non periodic)

Correlated

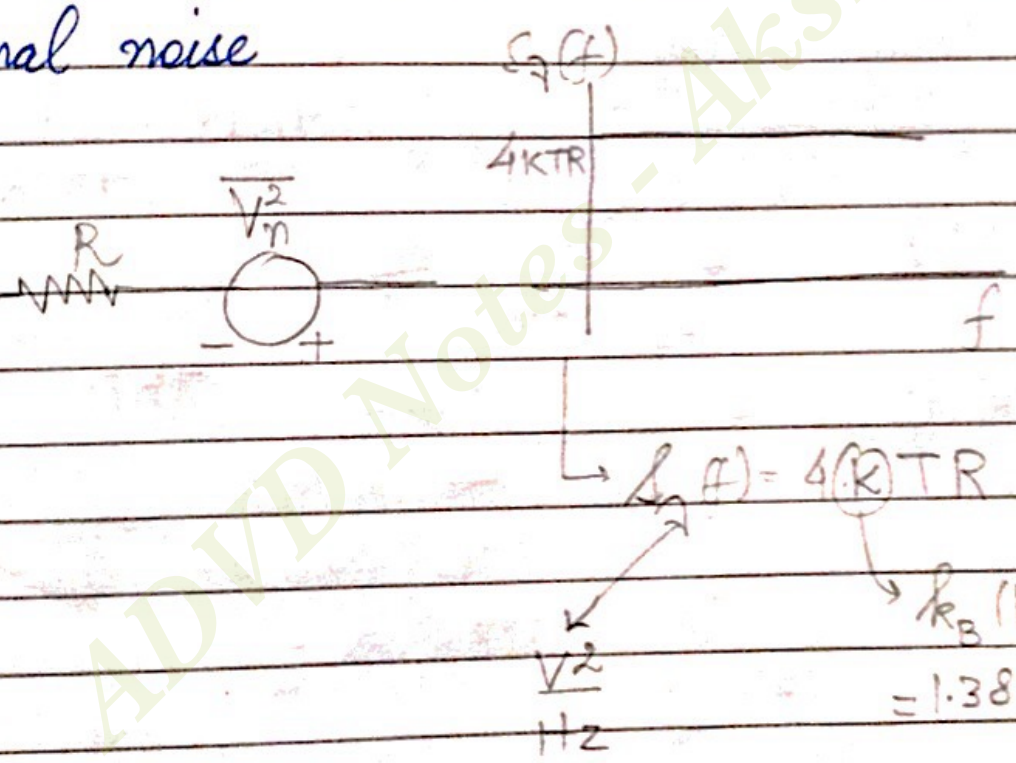
$$P_{avg}\Big|_{x_1+x_2} = P_{avg_1} + P_{avg_2} + \lim_{T\to\infty} \frac{1}{T}\int_{-T/2}^{T/2} 2x_1(t)\,x_2(t)\,dt$$

$\hookrightarrow = 0$ (if $x_1(t)$ & $x_2(t)$ are uncorrelated)

Uncorrelated

$$P_{avg} = P_{avg_1} + P_{avg_2}$$

• Thermal noise



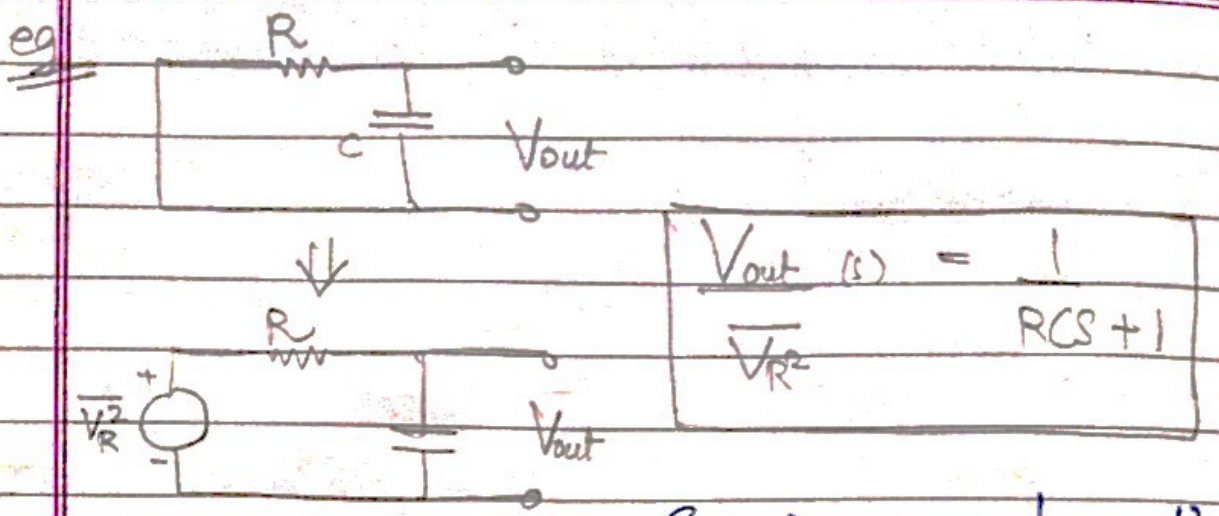
★ If $R = 50\,\Omega$

$T = 300$ K

$$\overline{V_n^2} = 4\times1.38\times10^{-23}\times300\times50$$
$$= 8.28\times10^{-19}\ V^2/Hz$$

$$\sqrt{\overline{V_n^2}} = 9.1\ nV/\sqrt{Hz}$$

eg



$$\frac{V_{out}(s)}{\overline{V_R^2}} = \frac{1}{RCs+1}$$

$$S_{out}(f) = S_R(f)\,|H(f)|^2$$

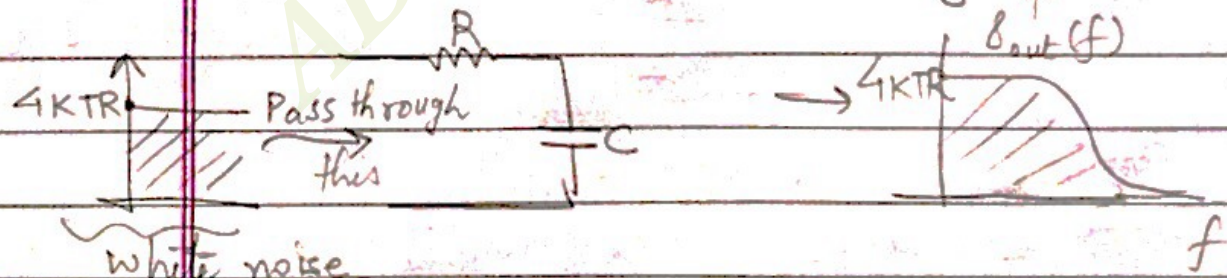
$$S_{out}(f) = 4KTR\left|\frac{1}{RCs+1}\right|^2_{s=2\pi jf}$$

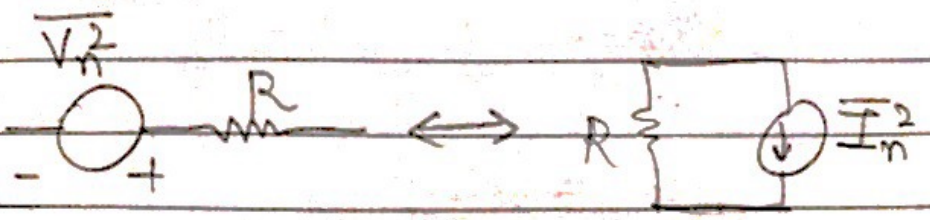
$$\Rightarrow S_{out}(f) = 4KTR\left[\frac{1}{4\pi^2R^2C^2f+1}\right]$$

$$P_{n,out} = \int_0^\infty S_{out}(f)\,df$$

$\Rightarrow P_{n,out} = \frac{KT}{C}$

- KT → Temp.
- C → Capacitance
- Boltzmann's const.
- $P \propto \frac{1}{C}$
- Power
- noise
- o/p



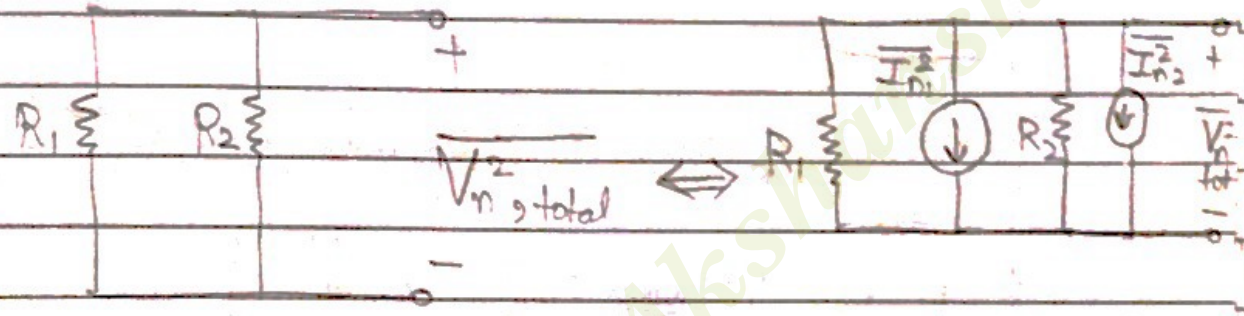


Ref^n :

$$\overline{V_n^2} = \overline{I_n^2} \times R^2$$

$$\Rightarrow \overline{I_n^2} = \frac{\overline{V_n^2}}{R} = \frac{4KTR}{R^2} = \frac{4KT}{R}$$

eg:



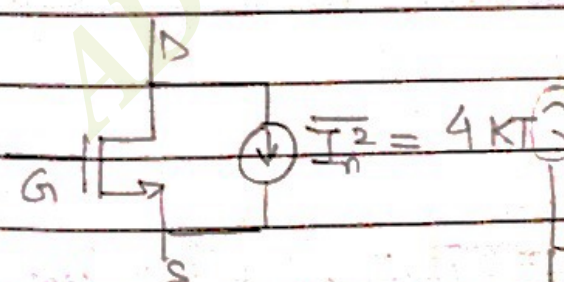
$$\overline{I_{n,total}^2} = \overline{I_{n1}^2} + \overline{I_{n2}^2}$$

$$= \frac{4KT}{R_1} + \frac{4KT}{R_2} = \frac{4KT}{(R_1 // R_2)}$$

$$\overline{V_{n,tot}^2} = \overline{I_{n,tot}^2} \times (R_1 // R_2)^2$$

$$= 4kT(R_1 // R_2)$$

eg:



$\overline{I_n^2} = 4KT\gamma g_m$

→ Its (nd) body effect coeff.

→ long channel transistors (> 1 μm) $= \frac{2}{3}$

→ short channel transistors ($\simeq 0.25$ μm) $= 2.5$

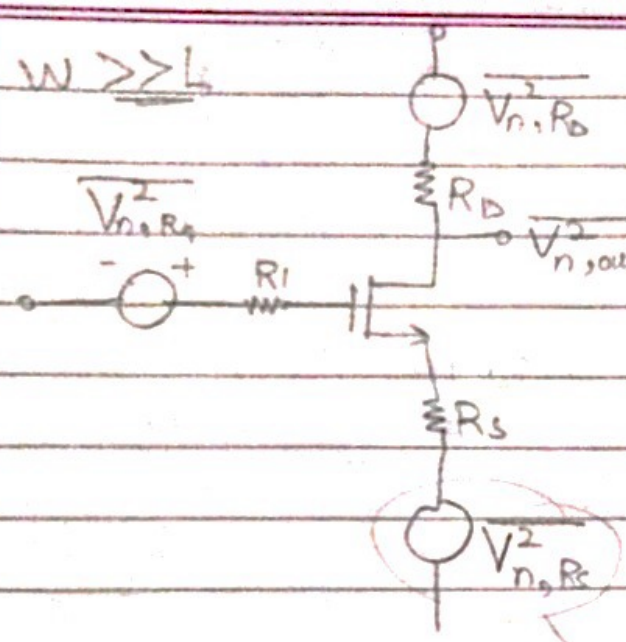
$\overline{V_n^2} = \overline{I_n^2} \times (r_o)^2$

r_o → resistance b/w drain & source

$= 4kT\gamma g_m r_o^2$

When $g_m \downarrow \Rightarrow \overline{V_n^2} \downarrow$

Q. $W >> L$



Distributed gate resistance

$R_1 = \frac{R_G}{3}$.

↳ if R_S, R_D can be neglected

$\overline{V_{n,R_S}^2}$ → noise voltage source (present with every resistance)

Process dependent const

$$\overline{V_{n,out}^2} = 4KT\left(\frac{R_G}{3}\right)(g_m r_o)^2$$

↳ Max. thermal noise in a transistor.

Flicker noise ⇒ 1/f noise

↳ $$\overline{V_{n,1/f}^2} = \frac{K}{C_{ox} WL} \cdot \frac{1}{f}$$

$K \to 10^{-25}\ V^2F$ (process dependent const)

↳ depends on device parameters & freq
↳ not found in resistances

* NMOS Current Source.

↳ Total noise = Thermal + Flicker
= Thermal + 1/f

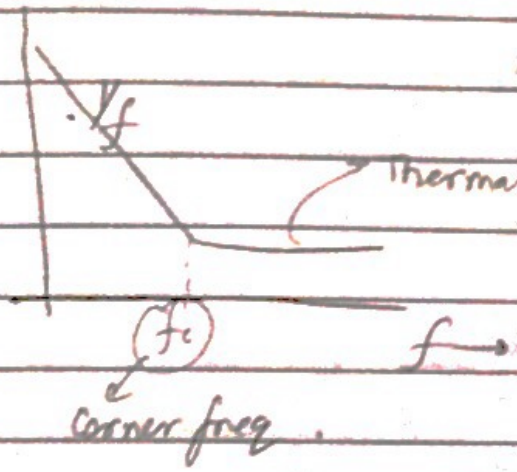
$$\overline{I_{n,total}^2} = \overline{I_{n,Thermal}^2} + \overline{I_{n,1/f}^2}$$

From flicker noise, we know $\overline{I_{n,1/f}^2} = \overline{V_{n,1/f}^2} \times g_m^2$

Thermal noise, $\overline{I_{n,Th}^2} = 4KT\left(\frac{2}{3}\right)g_m(f_2 - f_1)$

↳ (taking $f_1 = 1\,kHz$, $f_2 = 1\,MHz$)

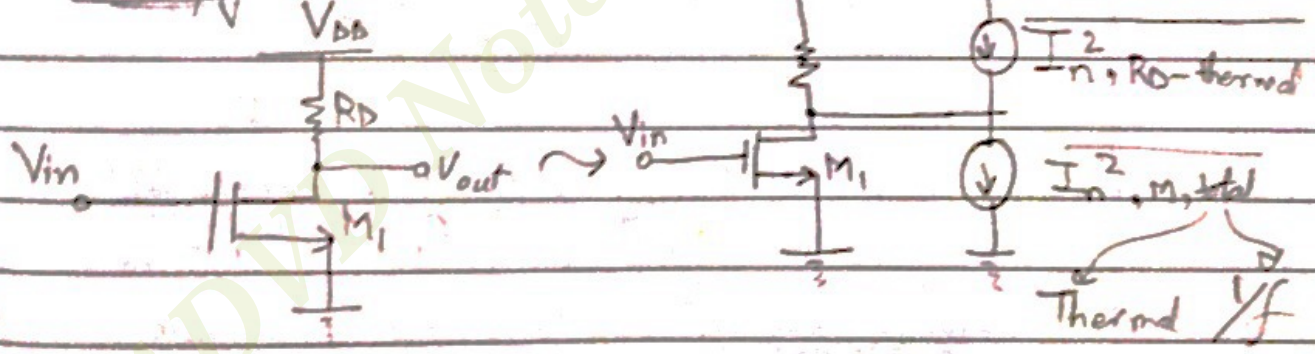
$\Rightarrow \int_{f_1}^{f_2} \overline{I_{n,1/f}^2}\, df = 6.91\, k\, \frac{g_m^2}{C_{ox} \cdot WL}$



$(4KT)\left(\frac{2}{3}g_m\right) = K' \frac{1}{C_{ox}WL} \frac{1}{f_c} g_m^2$

$\Rightarrow f_c = \frac{K'}{C_{ox}WL} \times \frac{3}{8KT} g_m$

✡ CS Config



$\overline{I_{n,RD,thermal}^2} = \frac{4KT}{R_D}$

$\overline{I_{n,M_1,thermal}^2} = 4KT\left(\frac{2}{3}\right)g_m$

$\overline{I_{n,M_1,1/f}^2} = \frac{k\, g_m^2}{C_{ox}\, WL} \times \frac{1}{f}$

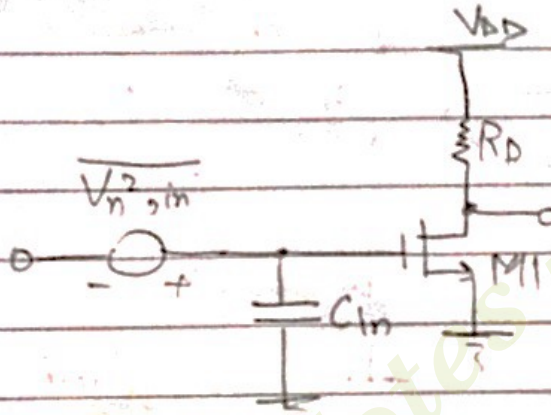
Let $(R_D \| r_o) = R_D$

$\overline{V_{n,out}^2} \longrightarrow \overline{V_{n,in}^2}$

depends on gain $\longrightarrow \dfrac{\overline{V_{n,out}^2}}{A_v^2}$

↳ If $R_D \ll r_o$,

$A_v = g_m R_D$



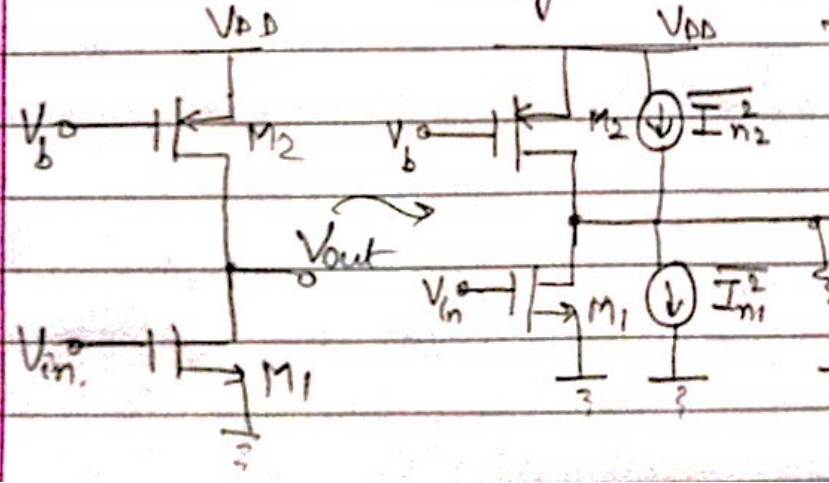
$\overline{I_{n,in}^2} = (C_{in}\omega)^2 \dfrac{4kT}{g_m^2}\left(\dfrac{2}{3}g_m + \dfrac{1}{R_D}\right)$

Technique to solve:-

1) Exclude $\frac{1}{f}$ noise
2) Get o/p voltage noise
3) Obtain a second represent^n for o/p voltage noise
4) Equate 2 expressions for o/p voltage noise
5) Determine i/p current noise

☆ Common Source Configur^n

Q *

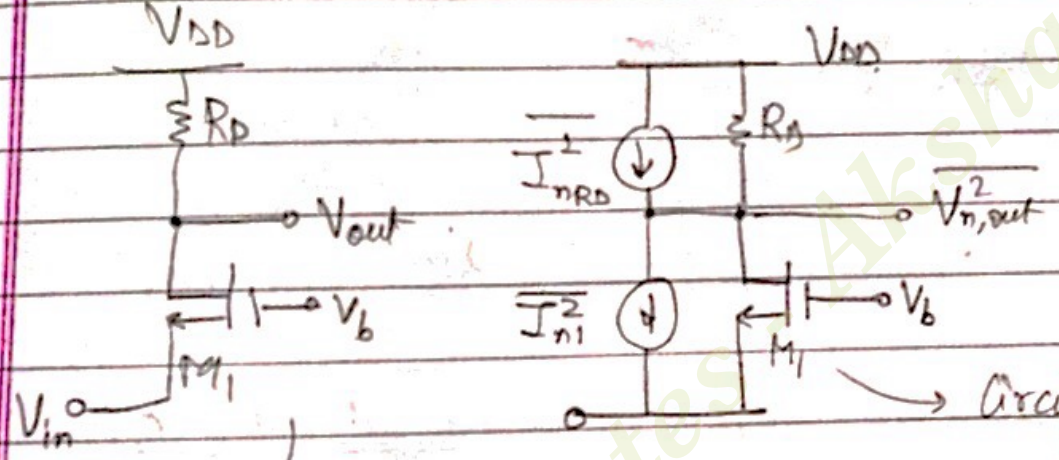


$$\overline{V_{n,out}^2} = 4kT\left(\frac{2}{3}g_{m1} + \frac{2}{3}g_{m2}\right)(r_{o1} \| r_{o2})^2$$

$$\overline{V_{n,out,total}^2} = \frac{2}{3}(g_{m1} - g_{m2})(r_{o1} \| r_{o2})\frac{kT}{C_L}$$

Signal to noise (SNR) ratio.

Common Gate Analysis



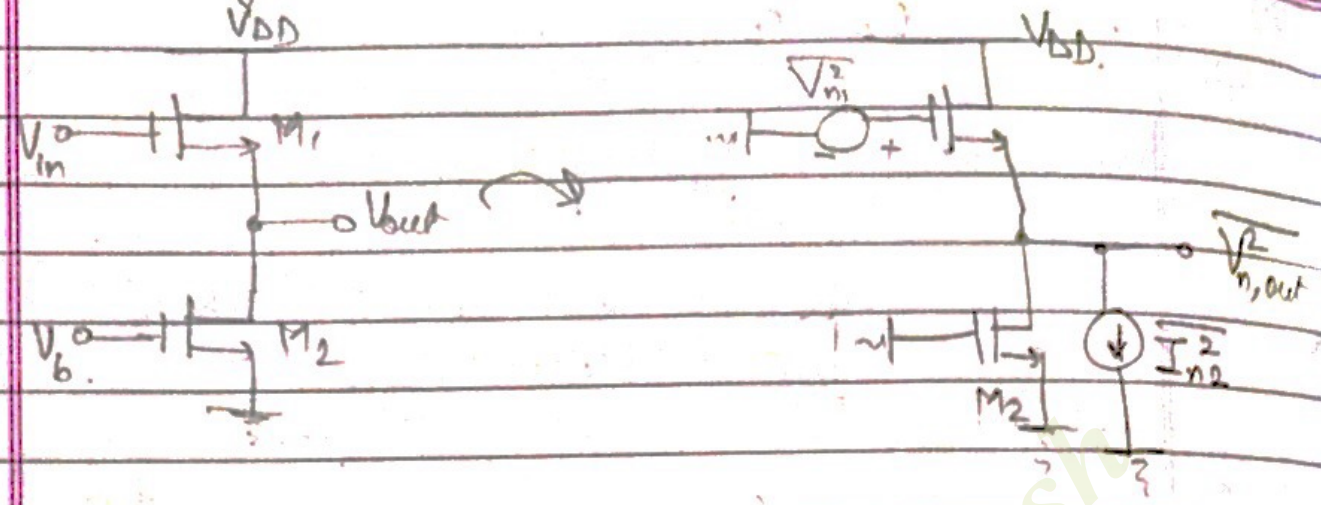
→ Circuit including noise.

→ Channel length modul^n neglected.

→ low i/p impedance ⇒ i/p referred noise cannot be neglected even at low freq$_s$.

$$\overline{V_{n,in}^2} = \frac{4kT(2g_{mb} + 1/R_D)}{(g_m + g_{mb})^2}$$

✱ Source follower



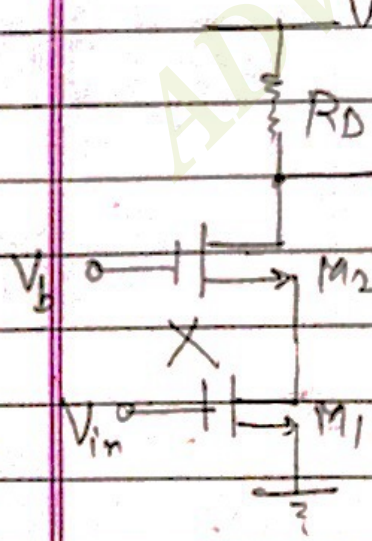
(Source follower circuit including noise)

Q. Given $\overline{V_{n,out}^2}$ due to M_2 & A_V

How do you get $\overline{V_{n,in}^2}$?

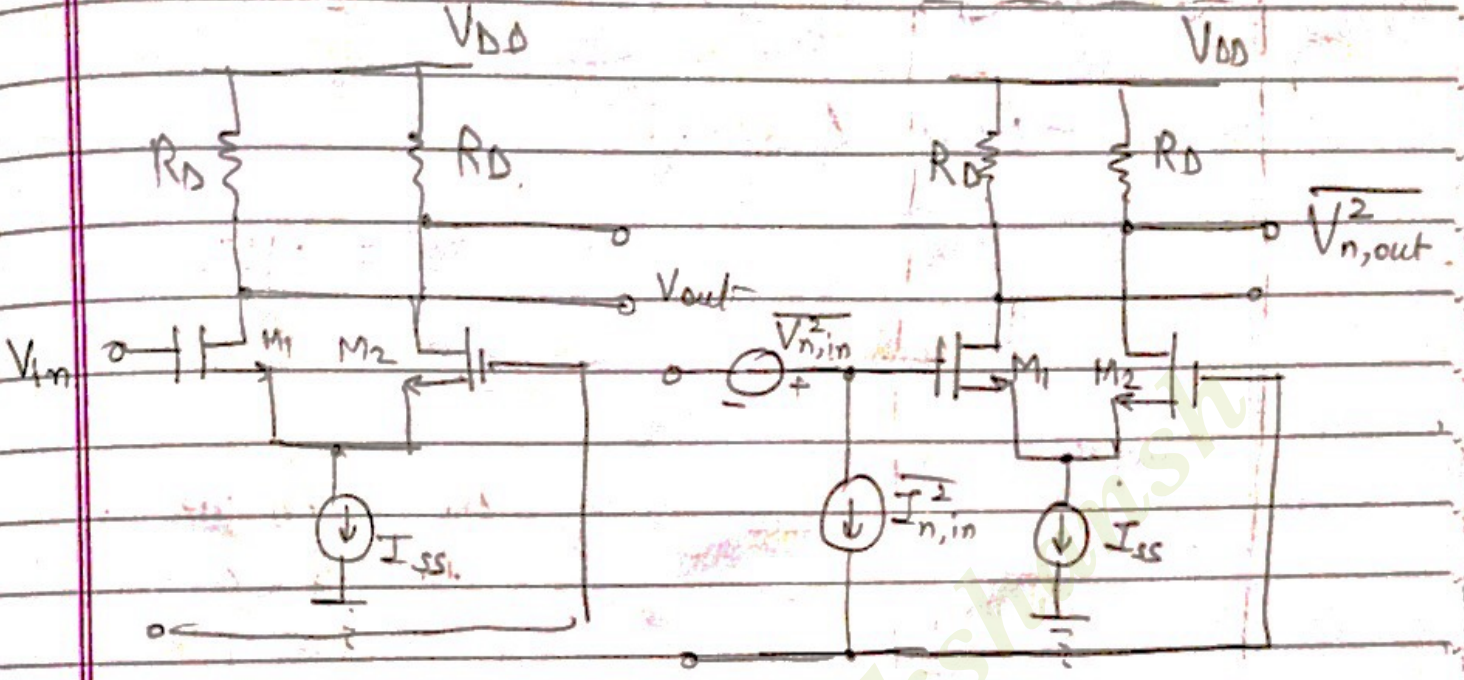
$$\overline{V_{n,in}^2} = \overline{V_{n1}^2} + \frac{\overline{V_{n,out\ due\ to\ M_2}^2}}{A_V^2}$$

✱ Cascode stage :-



- M2 with biasing, acts as current source
- Noise currents in RD & M2 adds up.
- ✓ The combined noise current flows through M2.
- ✓ Effectively a common source noise analysis

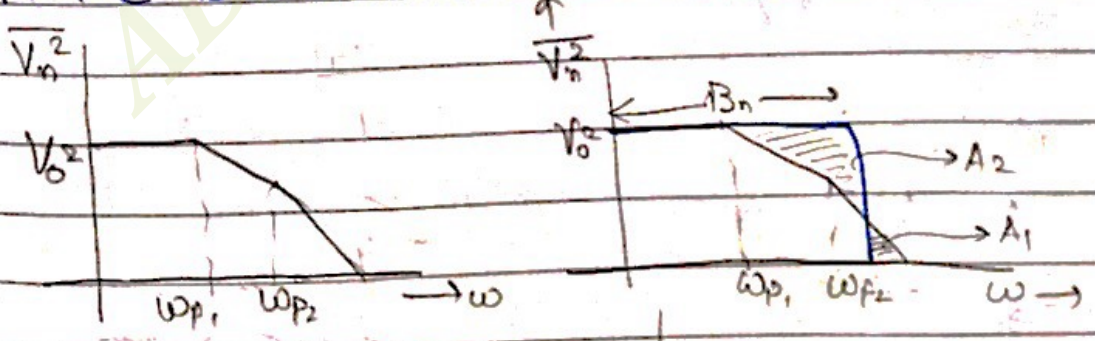
★ Differential Pair



$$\overline{V_{n,in}^2} = 8kT\left(\frac{2}{3g_m} + \frac{1}{g_m^2 R_D}\right)$$

$$\overline{V_{n,in,total}^2} = 8kT\left(\frac{2}{3g_m} + \frac{1}{g_m^2 R_D}\right) + \frac{2k}{C_{ox} WL}\left(\frac{1}{f}\right)$$

NOISE BANDWIDTH

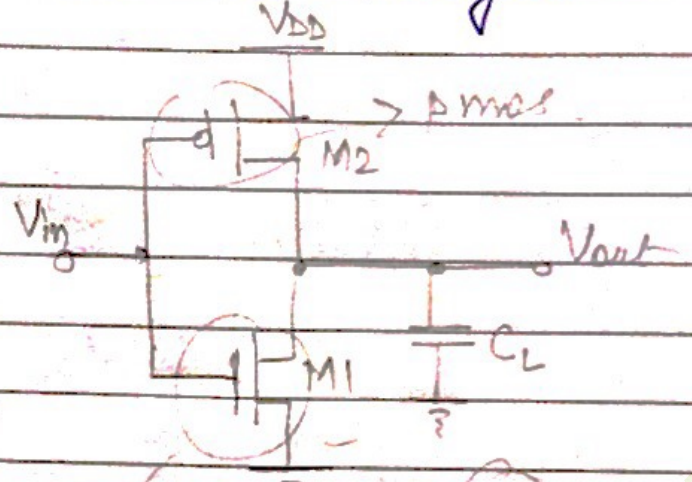


↳ If $A_1 = A_2$, then,

∴ $BW = V_o^2 \times B_n$

CMOS INVERTER

* First Order Analysis



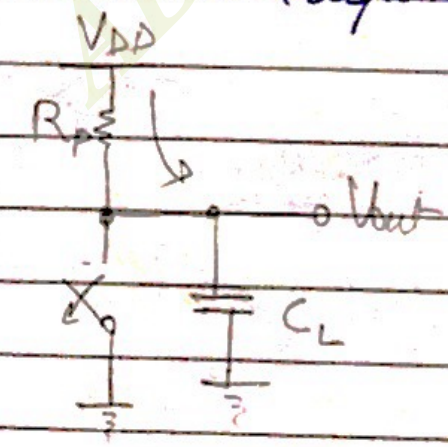
M1 = NMOS
M2 = PMOS

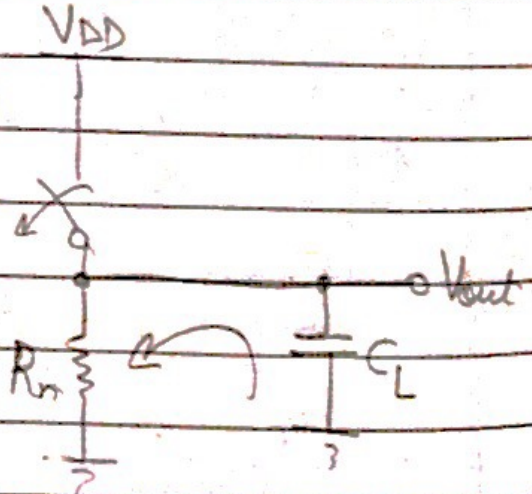
At high i/p :
NMOS becomes SC
PMOS " OC
0 = So, Vout gets to ground

At low i/p:
NMOS → OC.
PMOS → SC
1 = So, Vout = VDD.

→ Inverter.

* Transient response





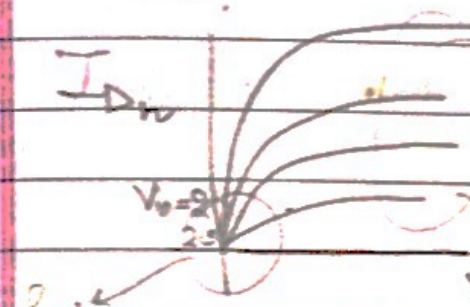
* low to high i/p o/p.

* high i/p to low o/p.

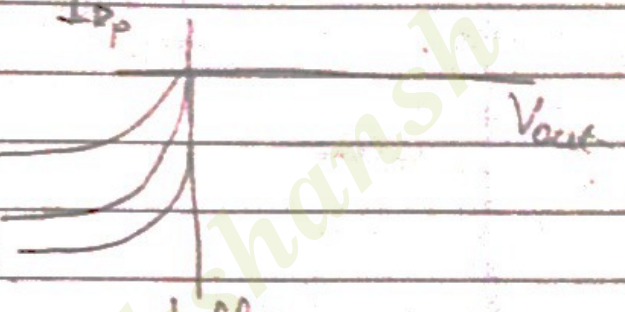
t_{PHL} = propagn delay High to low = $f(R_{on} \cdot C_L)$

$= 0.69\, R_{on} C_L$

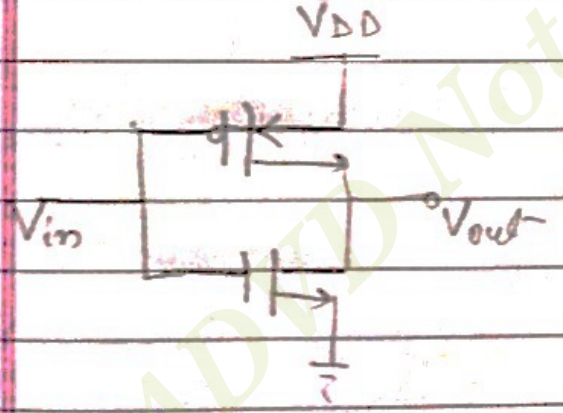
* NMOS

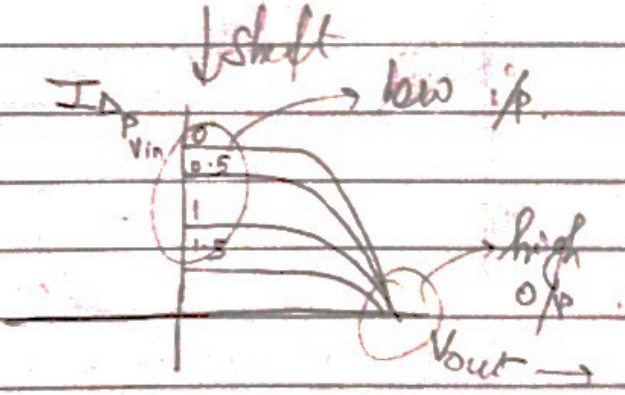


PMOS



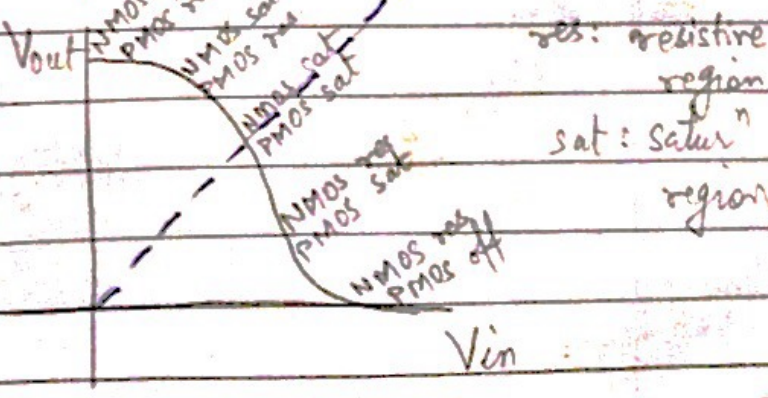
Chara for CMOS





* VTC : Voltage Transfer Characteristics:

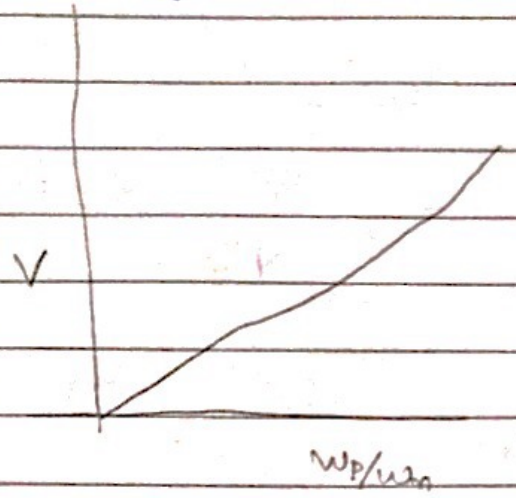
So, basically, for inverter.



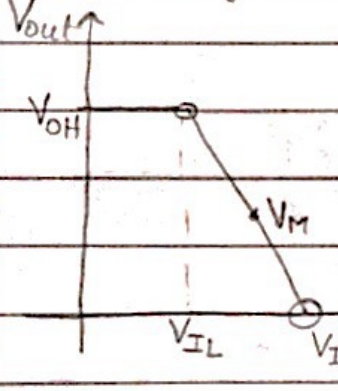
res: resistive region
sat: saturn region

★ VTC : Voltage Transfer Char.

★ Switching Threshold as a function of Transistor Ratio:



★ Determining V_{IH} & V_{IL}



Noise Margin (NM)

↳ $NM_{high} = V_{DD} - V_{IH}$

$NM_{low} = V_{IL}$

★ Gain as a fn of V_{DD}.

On the graph of Vout vs V_s, we see that we get ideal VTC (nearly), when V_s is low.

★ Char. in order to get a good device :-

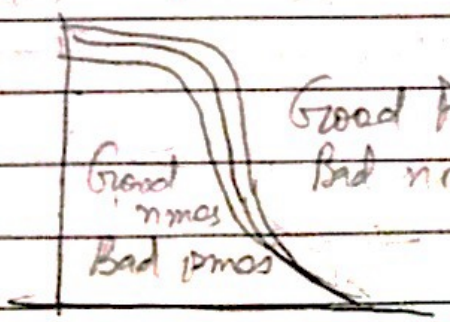
t_{ox} ↓

L ↓

W ↑

V_m ↓

⇒



* propag^n delay :

$$t_{PHL} \simeq \frac{C_L}{K_n V_{DD} \frac{W}{L}}$$

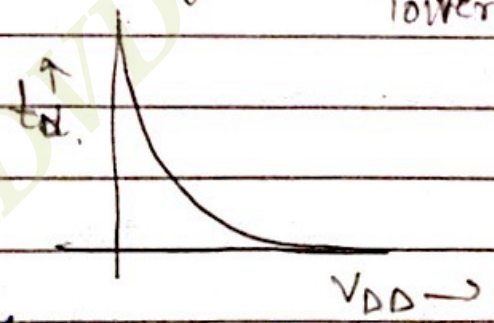
; capacitance $C_L \downarrow$ & $V_{DD} \uparrow$ to get lower propag^n delay.

* Design for Performance :
  - Keep capacitances small.
  - Increase transistor sizes
  - Increase V_{DD}.

* Power dissipation $\propto V_{DD}$

Now, it is seen that time delay $(t_d) \propto \frac{1}{V_{DD}}$

So, time delay $\propto \frac{1}{\text{Power dissipation}}$



* NMOS / PMOS ratio .

$$\beta = \frac{W_p}{W_n}$$

W_p → width of pmos

W_n → width of n mos

Way of designing:

Equal propagⁿ delay

① $t_{PHL} = t_{PLH}$.

↳ $\beta = \frac{W_p}{W_n} \simeq 2.4$

Unequal

② lowest t_p

$\beta = \frac{W_p}{W_n} \simeq 18$

Impact of rise time on propgⁿ delay.

Directly propⁿal.

* Dynamic Power Dissipation:

Energy transⁿ = $C_L * V_{DD}^2$

Power = $\frac{\text{Energy}}{\text{Transⁿ}} * f = C_L \times V_{DD}^2 \times f$

* Transistor sizing:

See fig from Razavi

* Minimizing short circuit of power.

* Static power consumption - - -

* Principles of power reduction:-

1) Reduce voltage

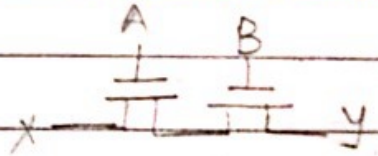
2) Reduce switching activity.

3) ~~Redu~~ Reduce physical capacitance.

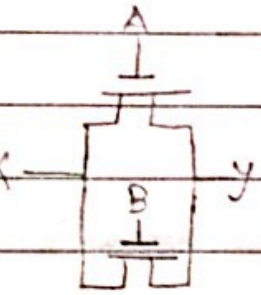
GATES

PUN : Pull Up Network = PMOS transistor
PDN : Pull Down Network = NMOS transistor

* NMOS Transistors in

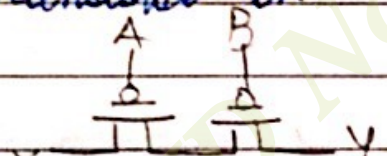
Series 

$Y = X$, if A AND B

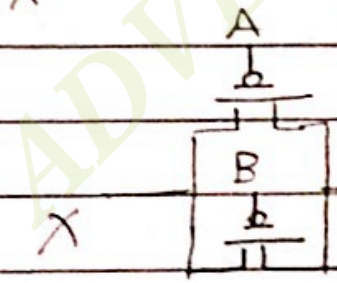
Parallel 

$Y = X$ if A OR B

* PMOS transistors in

Series 

$Y = X$ if $\overline{A}$ AND $\overline{B}$ $(= \overline{A+B}$ (de Morgans))

Parallel 

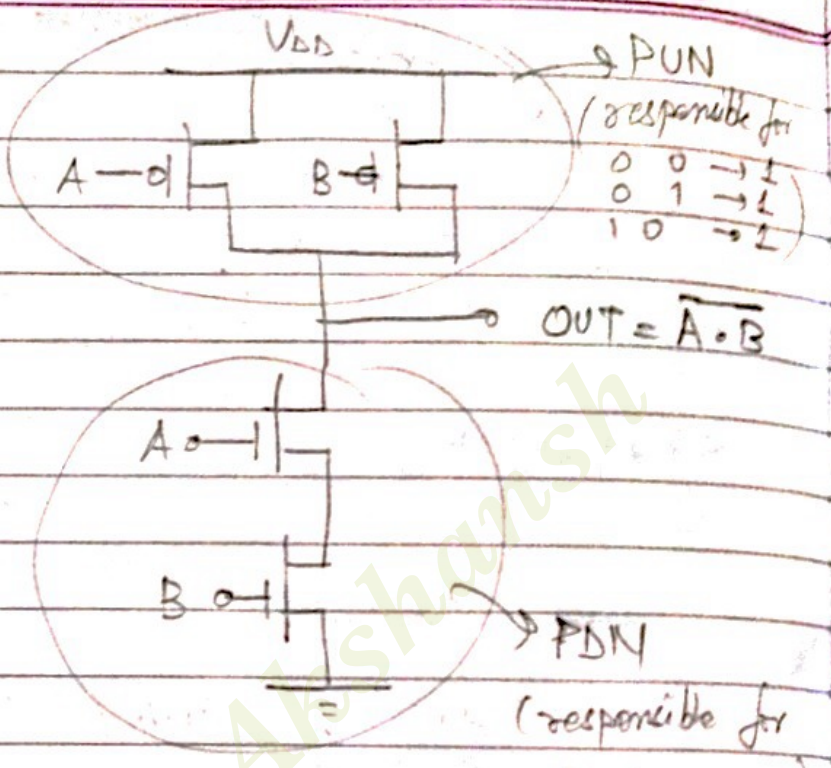
$Y = X$ if $\overline{A}$ OR $\overline{B}$ $(= \overline{A \cdot B})$

* o/p voltage swing ⇒ how much o/p can vary : from 0 to V_{DD} or less.

* PUN is a DUAL of PDN.

eg NAND Gate

A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0



When A = B = 1,
PDN is high & all o/p goes to ground.
So, o/p = 0.

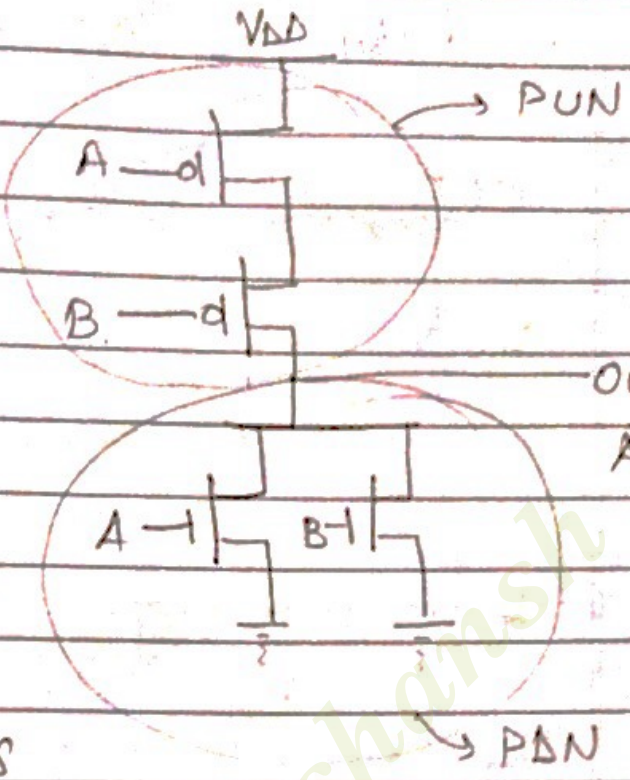
When either / both of A or B = 0,
PDN doesn't work. Only PUN works, making o/p = 1.
(when A = 0, B = 1 ⇒ $\overline{A}$ = 1, $\overline{B}$ = 0.
So, o/p is got as 1)

★ Steps to designing NOR / NAND gate :-

& vice versa
- If PUN is in series, PDN is in parallel.
- If one is NMOS, other will be PMOS.

eg NOR gate

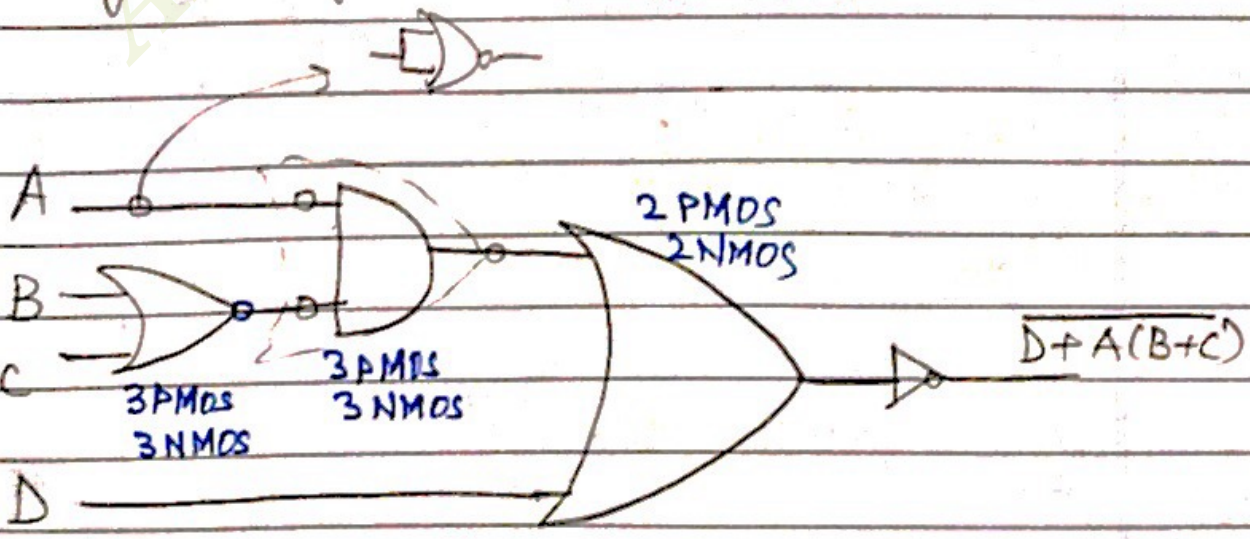
A	B	A+B
0	0	1
0	1	0
1	0	0
1	1	0



PUN : Series : PMOS
PDN : parallel : NMOS .

o/p = 1 when A = B = 0 . See PUN.
o/p = 0 when anyone of A or B = 1 . (o/p goes to ground — see PDN)

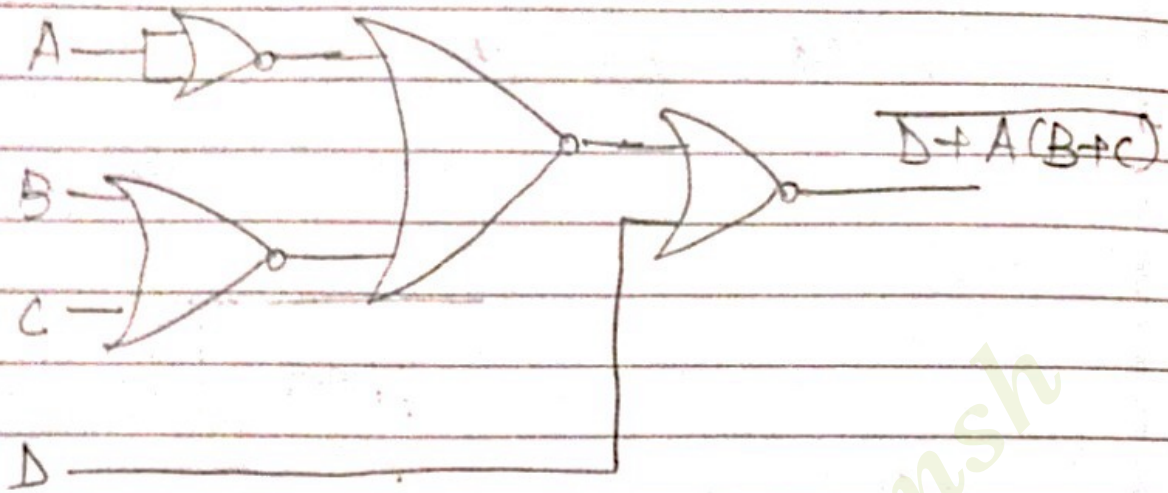
eg Consider implementⁿ of function
$OUT = \overline{D + A(B+C)}$
From Digital Design:



Total : 8PMOS, 8 & NMOS

Date
Page

Making all NOR gates :-



D	C	B	A	$\overline{D+A(B+C)}$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

o/p = 1 when A = 0

o/p = 1 when B = C = 0

& o/p = 0 when B = C = 1, B = 0, C = 1, B = 1, C = 0

o/p = 0 when D = 1

parallel.

Idea: o/p = 0 when D = 1 (OR) A(B+C) = 1

⇓

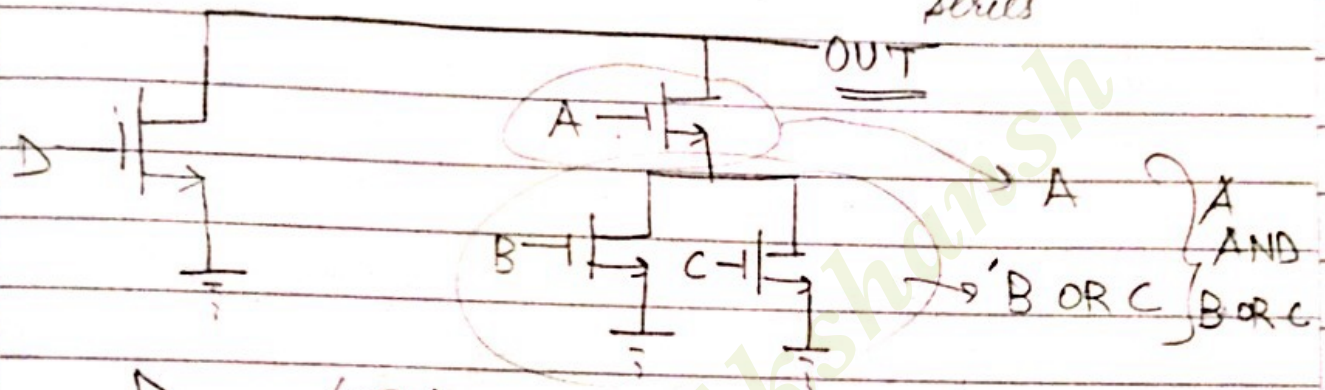
PDN

⇓

A = 1 AND (B = 1, C = 0 / B = 0, C = 1 / B = C = 1)

⇓

series



D (OR) A AND (B OR C)

D + A(B+C) → seeing o/p = 0

So, we are doing $\overline{D + A(B+C)}$.

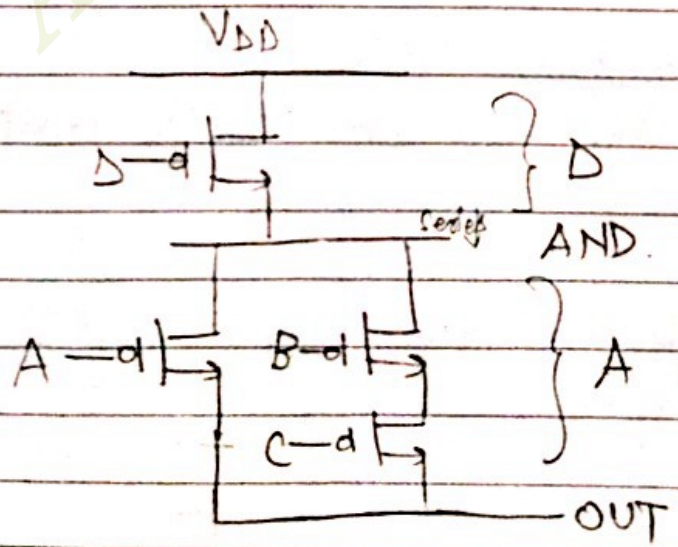
Now, seeing o/p = 1 ⇒ PUN

That is possible when

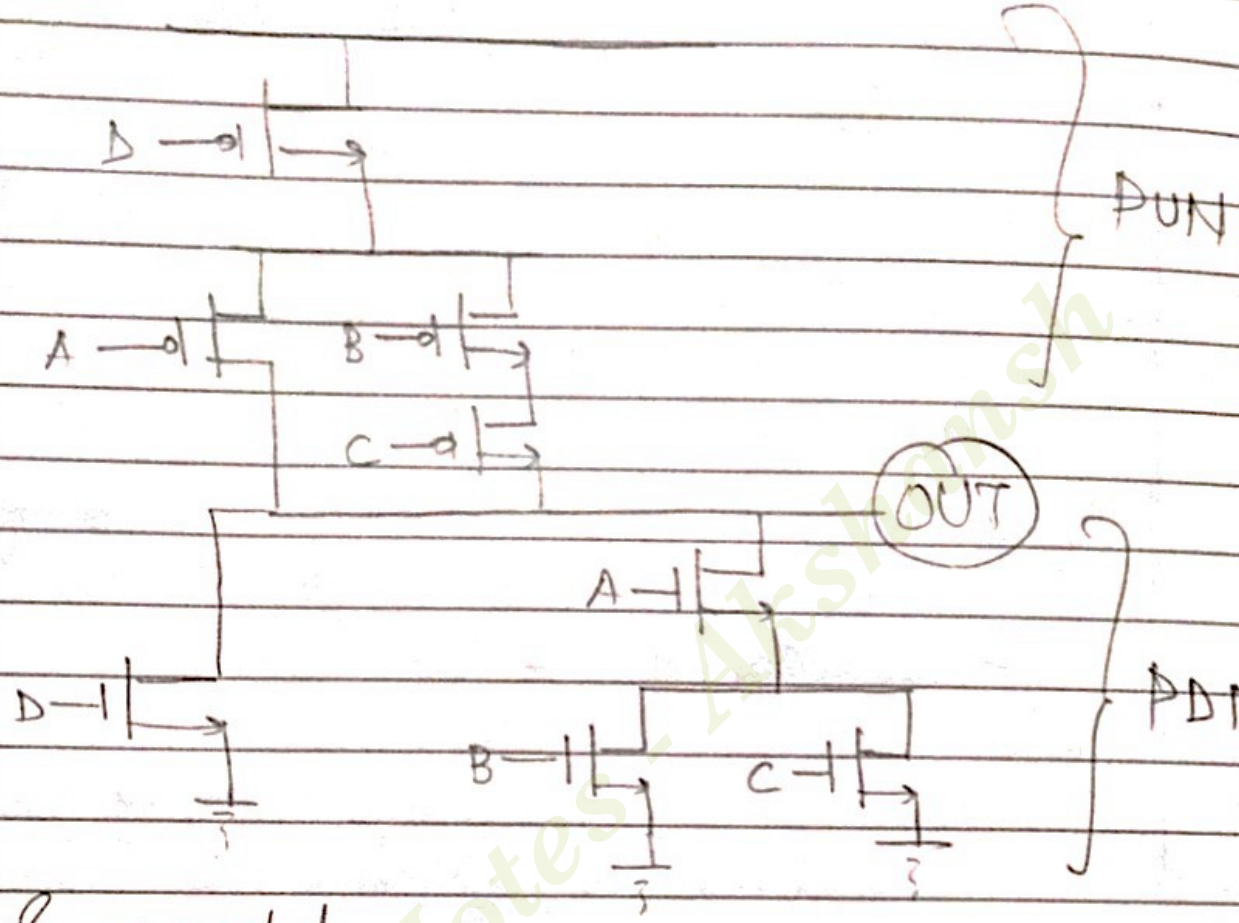
D = 0 (AND) A = 0.

(OR)

(B = 0 AND C = 0)



Combining both PUN & PDN :-

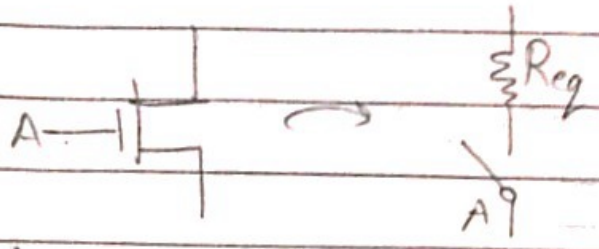


So, we needed
4 PMOS, 4 NMOS

☆ Properties of complementary CMOS Gates :

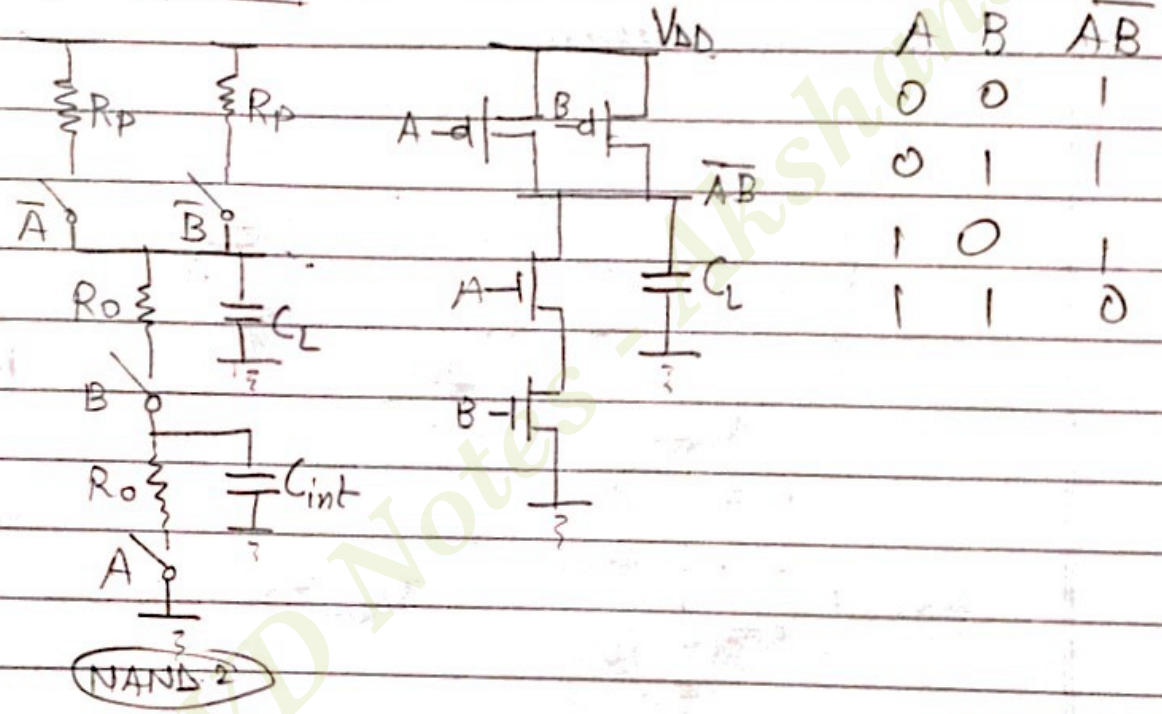
- High noise margins
  V_{OH} & V_{OL} are at V_{DD} & GND resp.
- No static power consumption
  There never exists a direct path b/w V_{DD} & V_{SS} (GND) in steady state mode.
- Comparable rise & fall times.

SWITCH DELAY MODEL.



✓ Models for
NAND2, INV, NOR2

NAND GATE



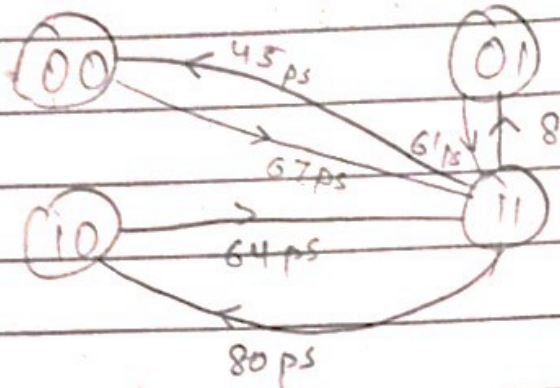
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

• Delay dependence on i/p patterns

i/p data pattern	Delay (psec)
A = B = 0 → 1	67
A = 1, B = 0 → 1	64
A = 0 → 1, B = 1	61
A = B = 1 → 0	45
A = 1, B = 1 → 0.	80
A = 1 → 0, B = 1	81

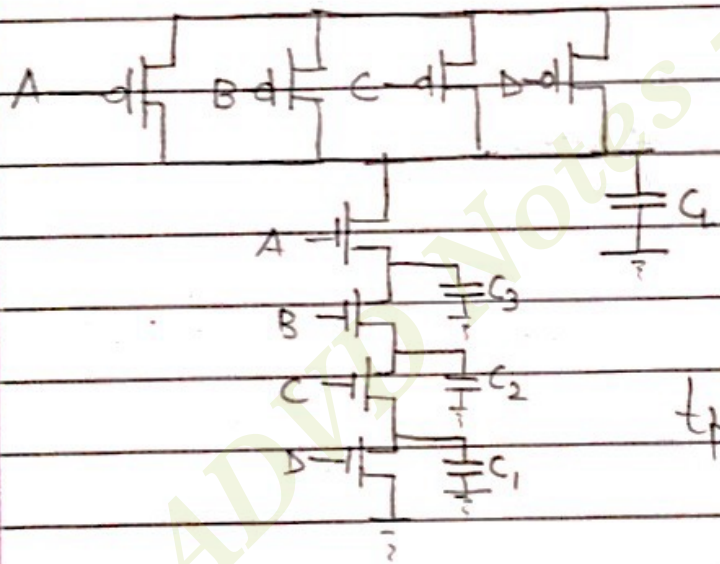
; NMOS = 0.5μm / 0.25μm
PMOS = 0.75μm / 0.25μm
C_L = 100fF

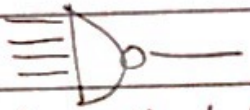
Making state chart



So, we find a lot of variation in propagⁿ delay.

* Fan-in considerations :-



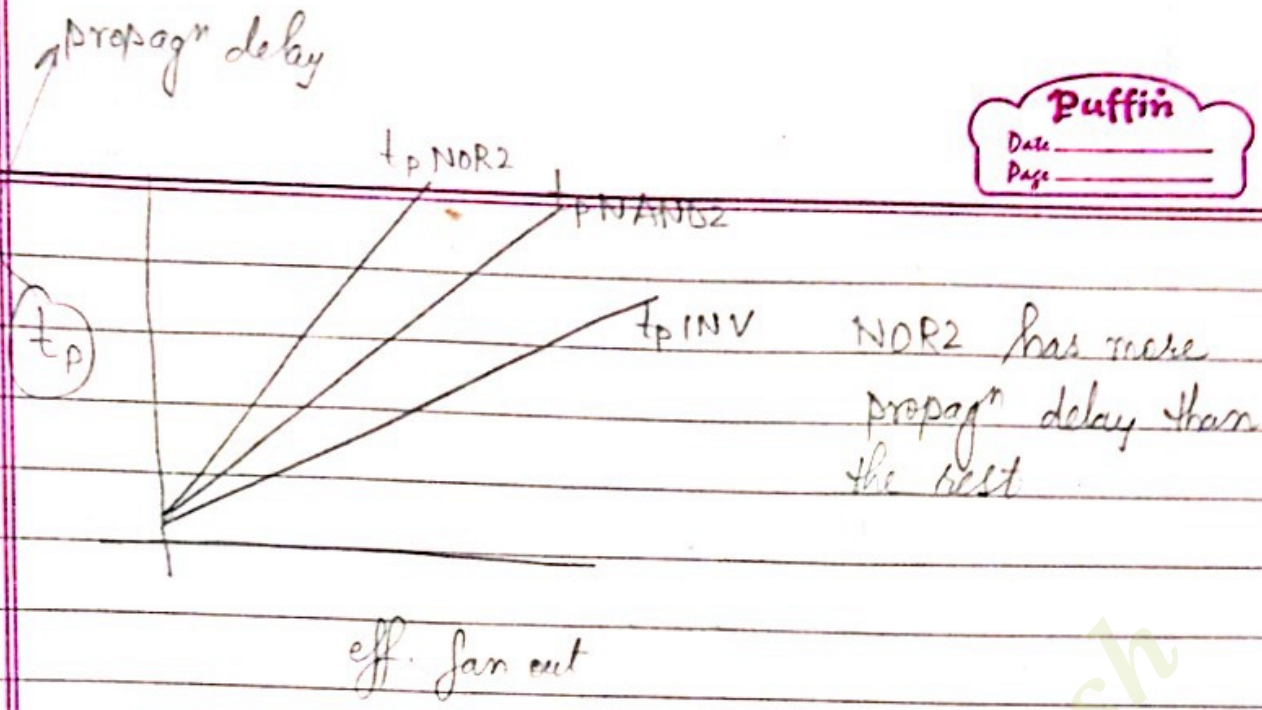


Distributed RC model (Elmore Delay)

$$t_{PHL} = 0.69 R_{eqn}(C_1 + 2C_2 + 3C_3 + 4C_4)$$

Q Why do I use 2 i/p NAND gate over 4 i/p NAND gate?
4 i/p NAND gate has more delay, even though 2 i/p NAND gate has more stages/levels.

* fan in : how many gates can feed in by current gate.
↳ gates with fan-in > 4 should be avoided.

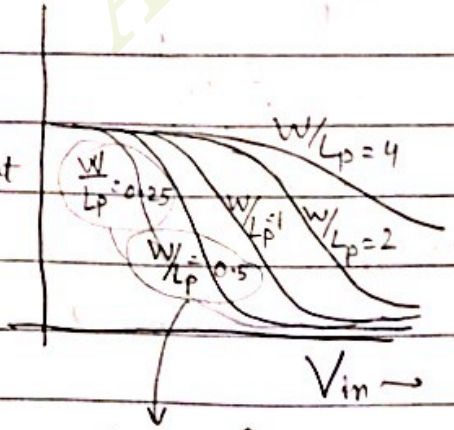


NOR2 has more propag^n delay than the best

* **Fast Complex Gates : Design Techniques.**

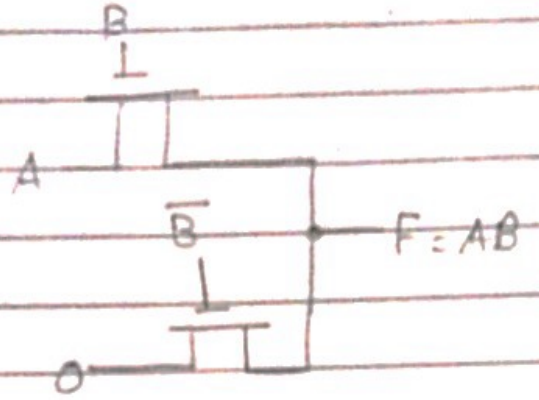
✓ Transistor sizing :- used as long as fan out cap. dominates
✓ Progressive sizing :- reduces delay by 20%
✓ Alternative Logic Structures.

- **Pseudo NMOS VTC**



Unusual case.
$\therefore$ $W < L_p$
Usually, $W > L_p$: always.

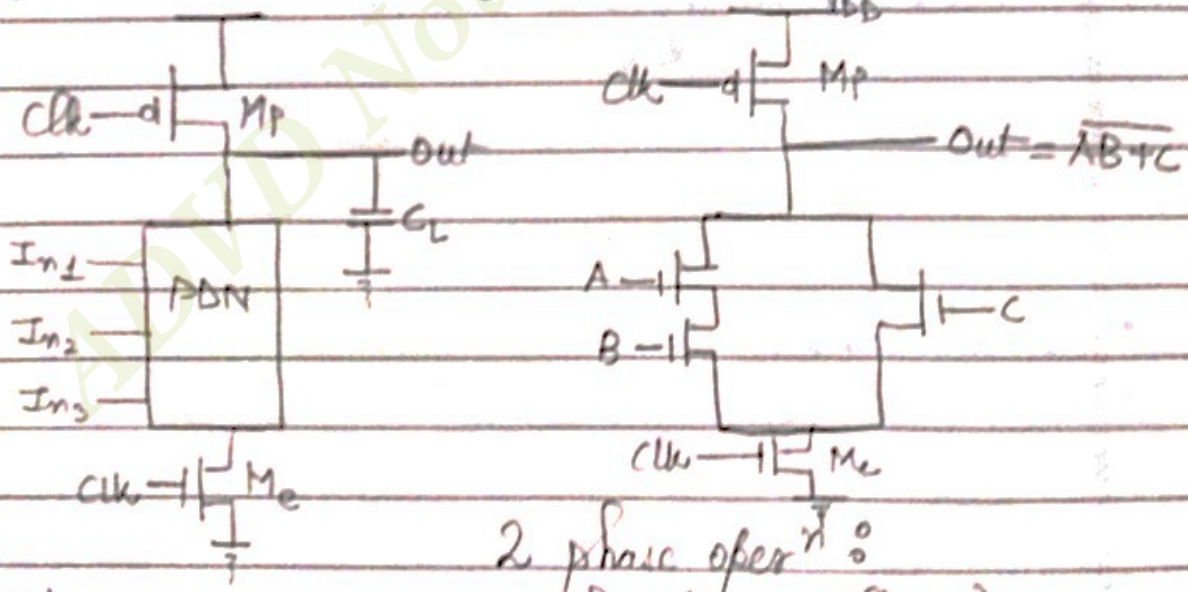
Q: Consider following AND gate (make without using PMOS)



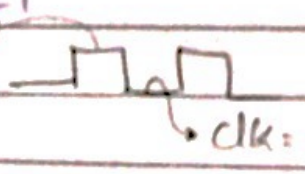
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

A = B = 0, lower part is connected, upper part is OC → goes to 0

* Dynamic CMOS Design :-



2 phase operation:
Precharge (Clk = 0)
Evaluate (Clk = 1)



- Properties of Dynamic Gates (self)

Seeing the circuit we find:

- Only one PMOS transistor. So, no. of PMOS reduced ⇒ charging time reduced
- When $clk_1 = 0$, it's active low, so it's ON. So, o/p = high (& clk_2 = OFF)
- When $clk_1 = 1$, it's OFF & clk_2 = ON

→ for o/p = low :

A AND B is high OR C is high

So, truth table for high o/p

A	B	C	o/p
1	1	0	low
1	1	1	↑
0	0	1	⋮
0	1	1	⋮
1	0	1	↓
			low

→ for o/p = high :

$\bar{A}B + C$ = low. So,

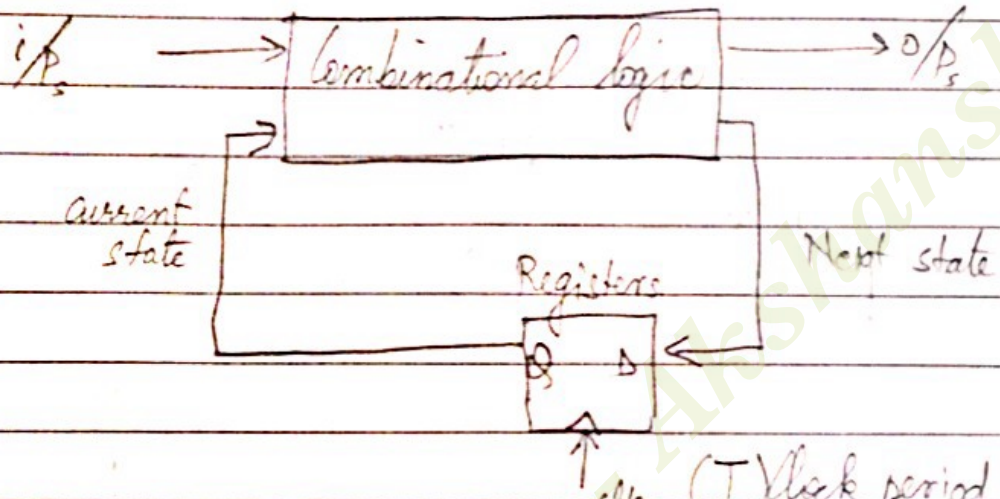
C = low OR A → low & B - low
A - high & B - low
A - low & B - high

↳ remaining combinations where o/p = low.

Puffin
Date 3/12/13
Page

Sequential Logic

= combinational logic + f/b.



(T) Clock period $> t_{cq} + t_{p\,logic} + t_{su}$

t_{su} → setup time

☆ Latch vs. Register

- **Latch :** Stores data when clock is low
- **Register :** Stores data when clk is high.

rises

☆

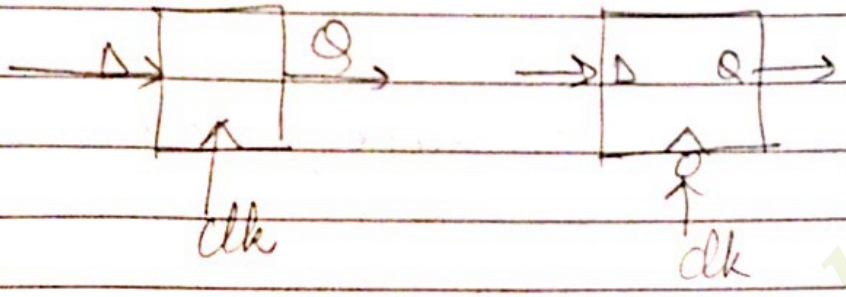
$$T > t_{cq} + t_{p\,logic} + t_{su}$$

t_{cq} → propag^n delay

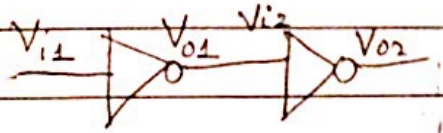
$$t_{ccd}\ \text{register} + t_{cd}\ \text{logic} \geq t_{hold}$$

t_{ccd} → contamination delay

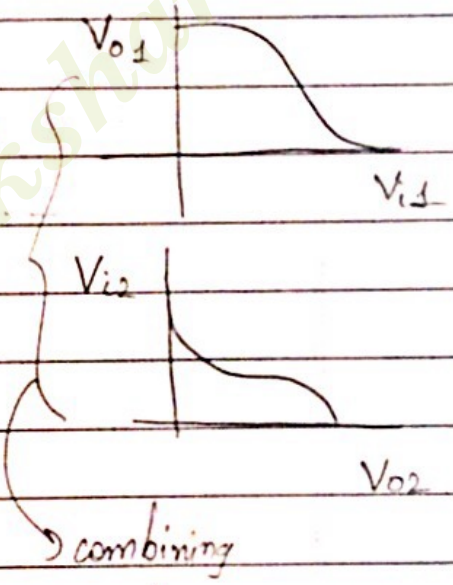
Latches → +ve latch & -ve latch.

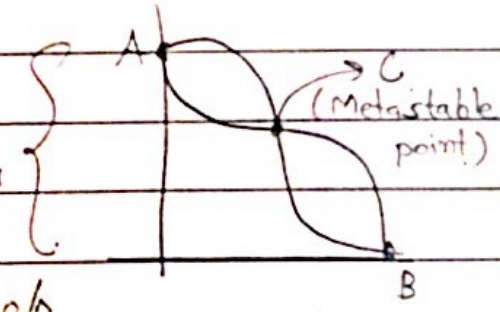


✱ Consider 2 cascaded inverters:



$V_{i1} = V_{o2}$ & $V_{o1} = V_{i2}$

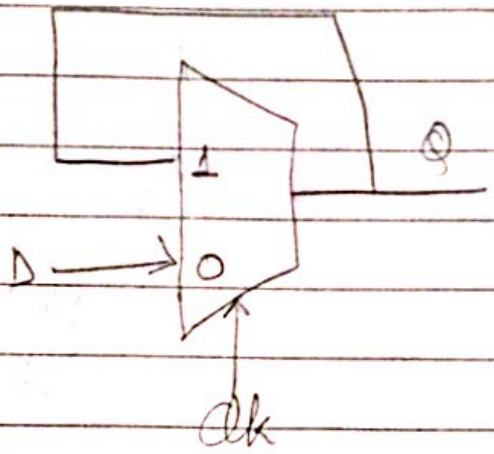




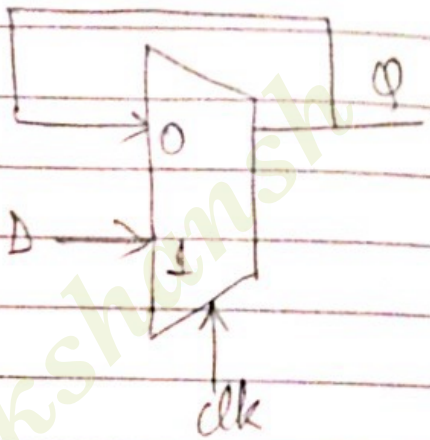
If V is at pt. C, sys. is stable. At all other pts, o/p goes to A or B pts

MUX Based Latches

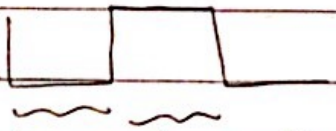
Negative Latch
(transparent when clk=0)

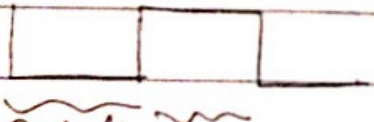


Positive latch
(transparent when clk=1)

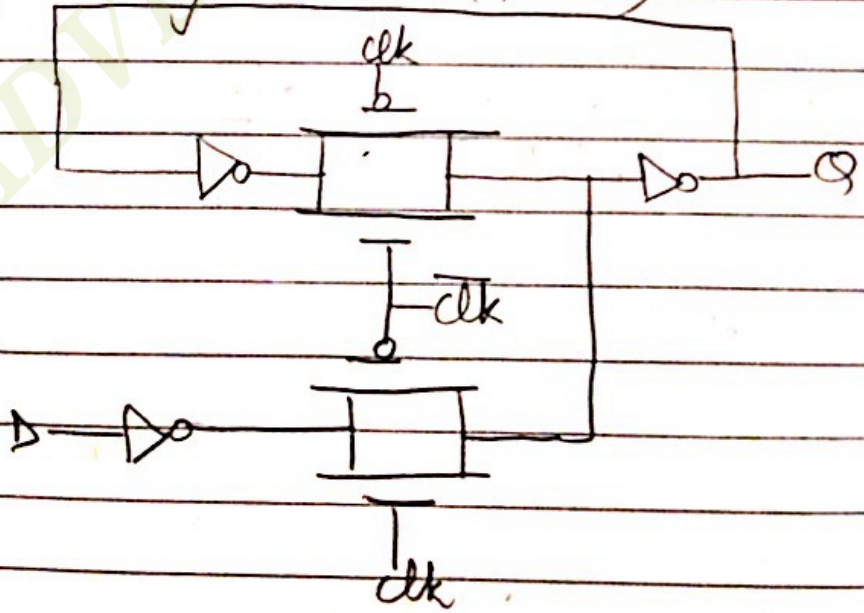


clk :-

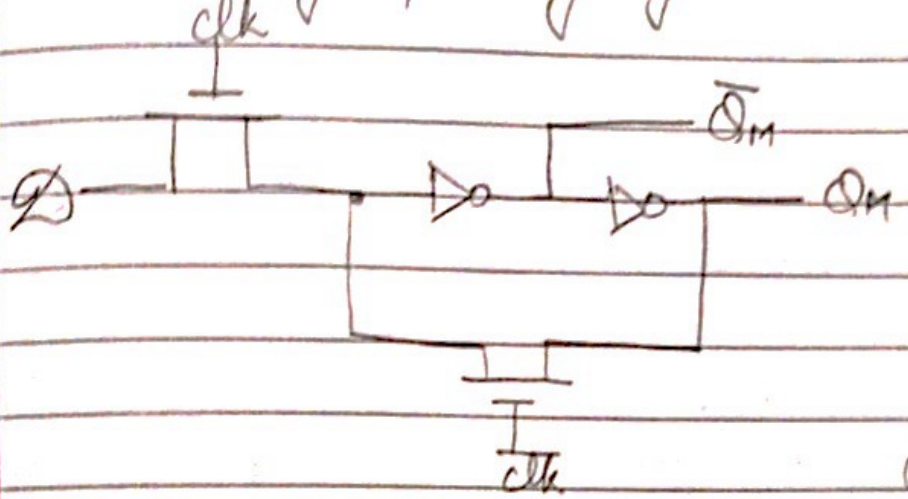




MUX :- (using NMOS & PMOS)



Another way of designing: (NMOS only)

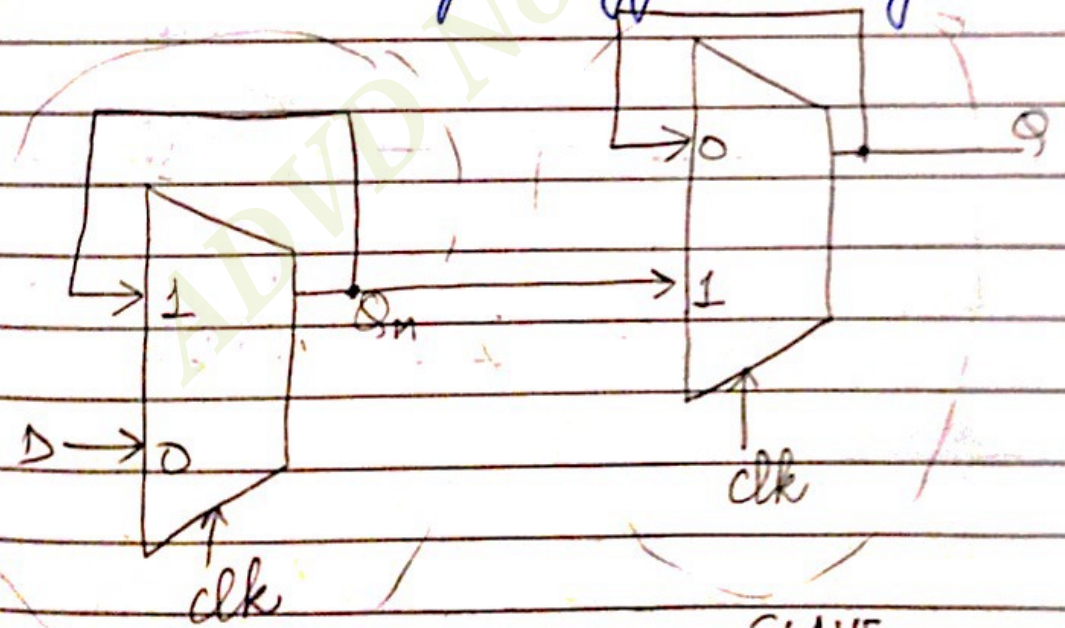


clk :

$\overline{clk}$:

→ may not be generated ideally. So, ∃ some delay always.

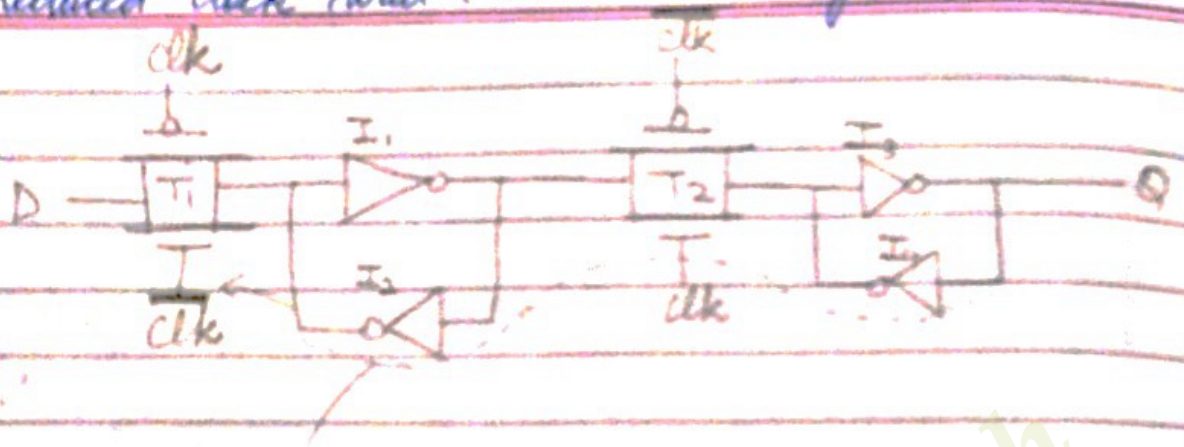
✡ Master-Slave (Edge-Triggered) Register.



MASTER (-ve triggered)

SLAVE (+ve triggered)

• Reduced clock load (Master slave Register)

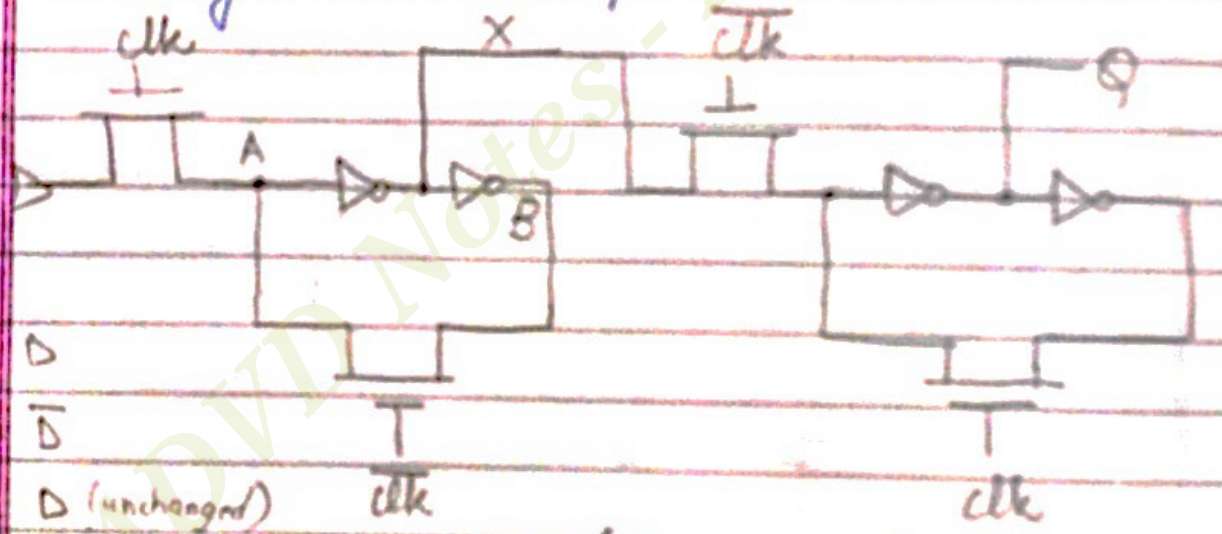


kind of feedback results if system is improper

"Clock Overlap" Occurs.

clk = $\overline{clk}$ = 1 or 0

• Avoiding Clock Overlap



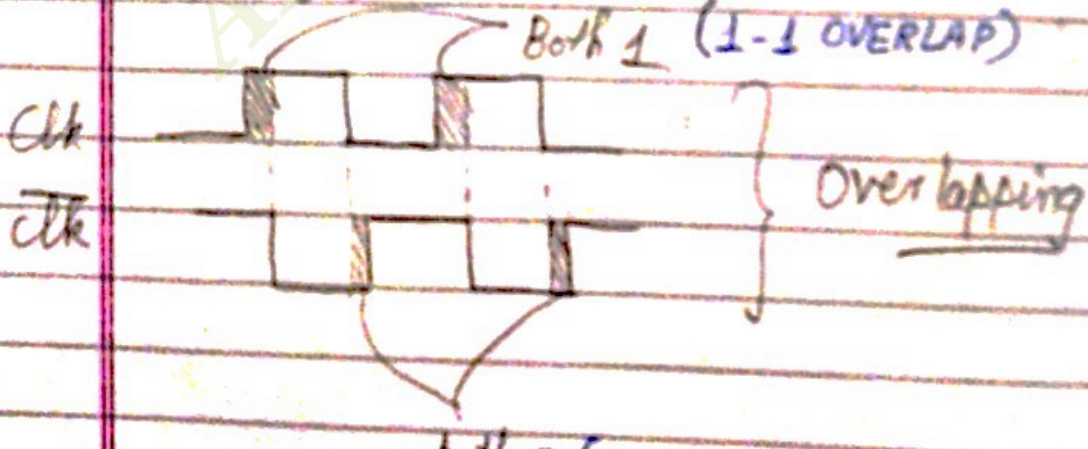
* Eqn:

A = D

B = A = D

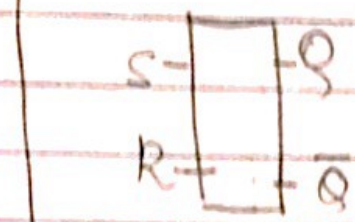
X = $\overline{A}$ = $\overline{D}$

Q = $\overline{X}$ = D (unchanged)



☆ Flip Flops

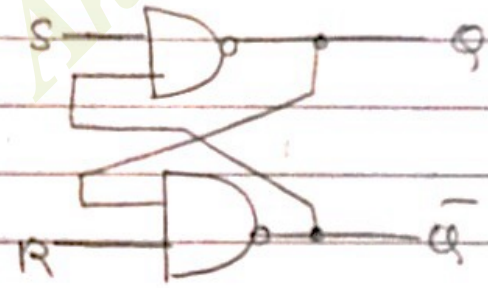
☆ SR Flip Flop



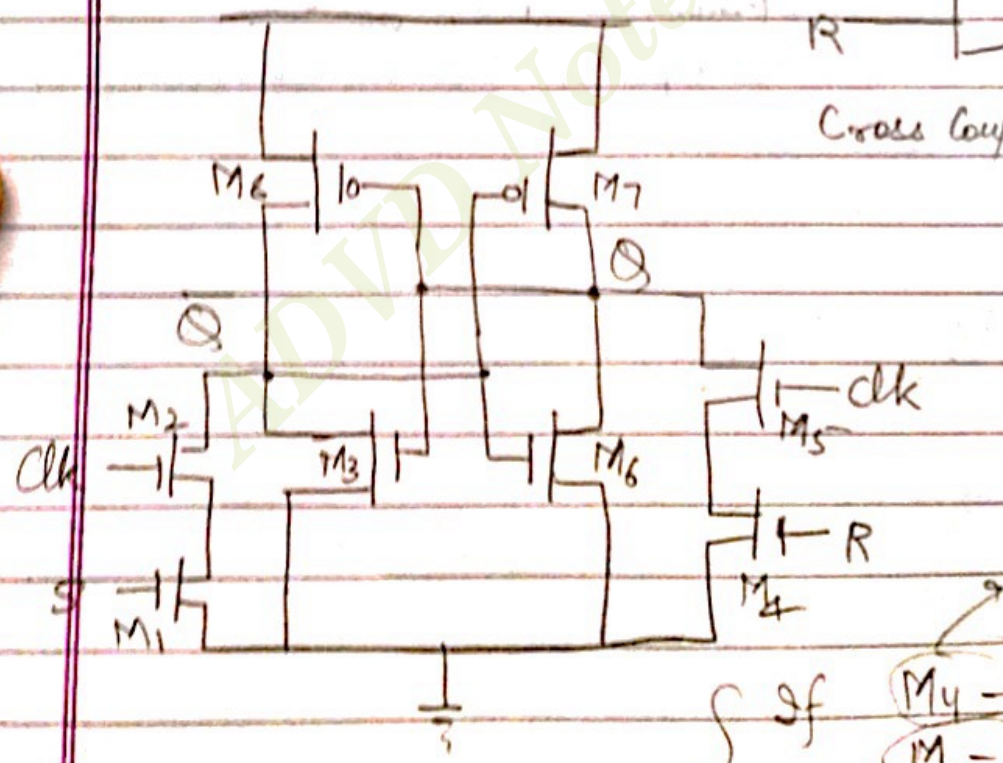
or → using NOR gates
using NAND gates

remains in previous state

S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
1	0	1	0
0	1	0	1
1	1	0	0



Cross Coupled NAND

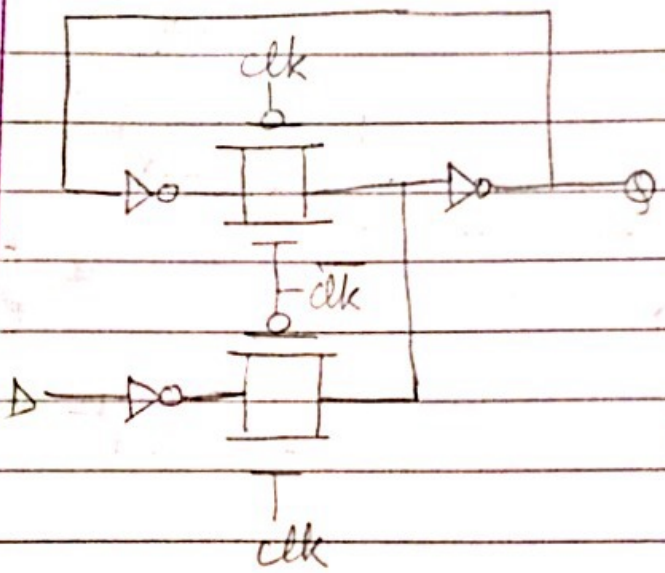


If R=1, clk=1
M_4 - SC & M_5 - SC
M_1 - OC, M_2 - SC
S=0.
clk is high

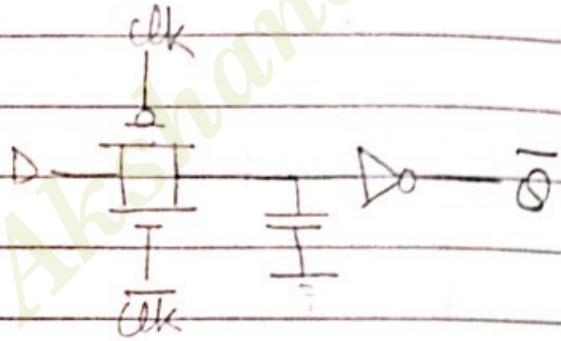
∴ S=0, R=1, we get Q=0, $\bar{Q}$=1

☆ Storage Mechanisms

Static



Dynamic.
(charge - based)



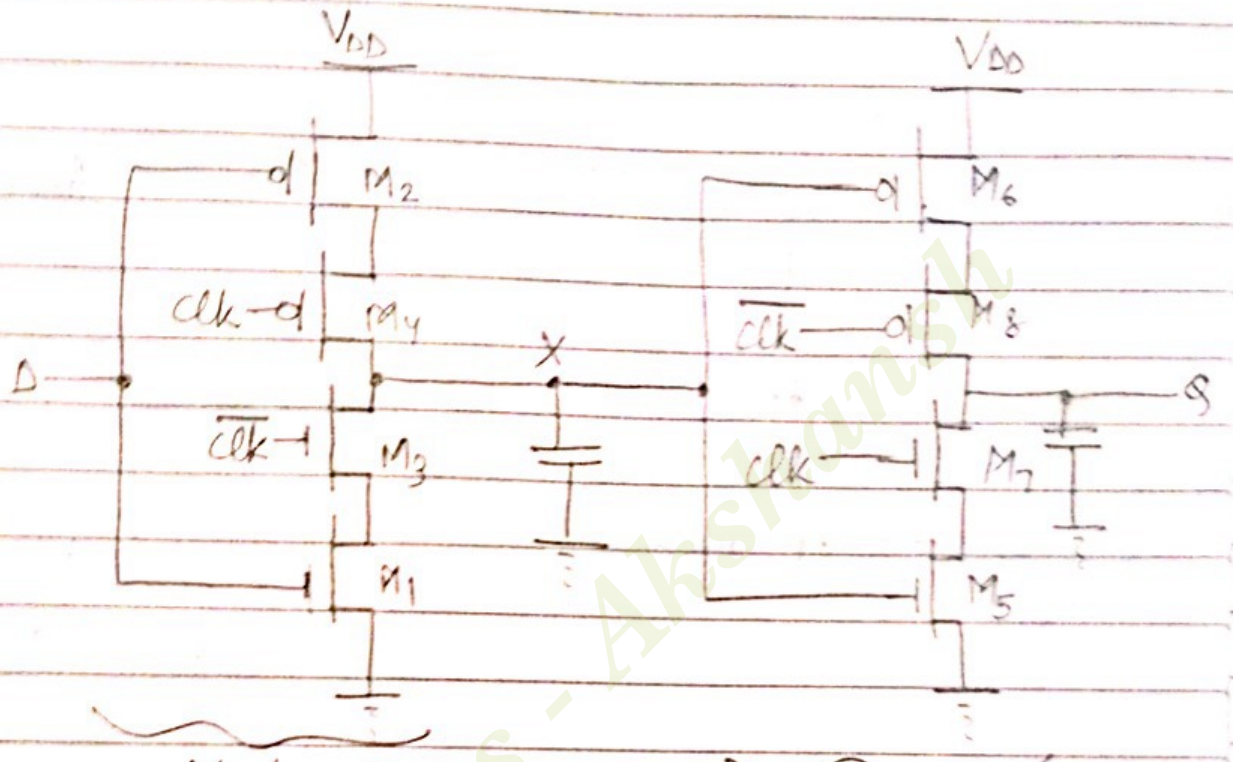
clk = 0 ⟶ D charges capacitance

If D = 1 ⟶ Capacitance charged to high (Capacitance previously discharged)

$\Rightarrow \overline{Q} = 0$

D_{n+1}	D_n
0	0
0	1
1	0
1	1

• Other Latches / Registers : C^2MOS :



M_1 & M_2 act as inverter.
If M_3, M_4 → SC
⇩
clk = 0
⇩
X = $\overline{D}$ (Capacitor charges)

X is not transferred to Q
Q remains same as before

M_5, M_6 act as Inv
If M_7, M_8 → SC
⇩
clk = 1
⇩
Q = $\overline{X}$ = $\overline{\overline{D}}$ = D

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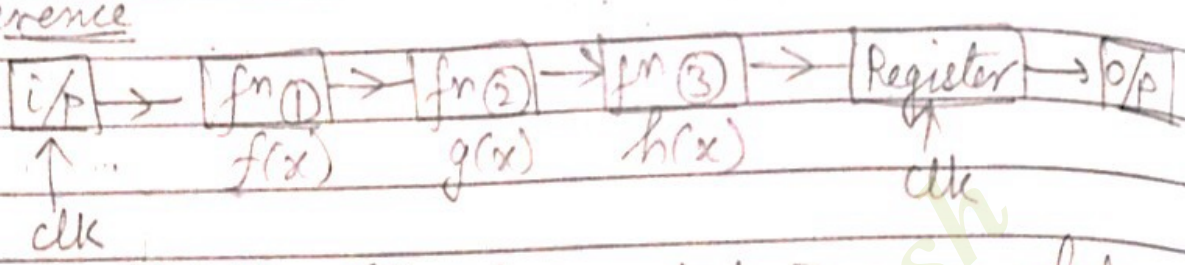
* Pipelining :

Parallelising

Reference

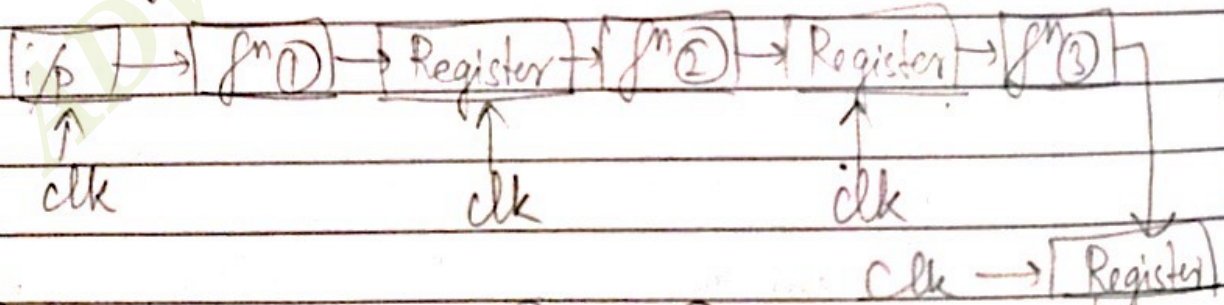


fns ① → ③ get executed in every clock pulse

Clk period	fn ①	fn ②	fn ③
1	f(x)		
2		g(f(x))	
3			h(g(x))
⋮			

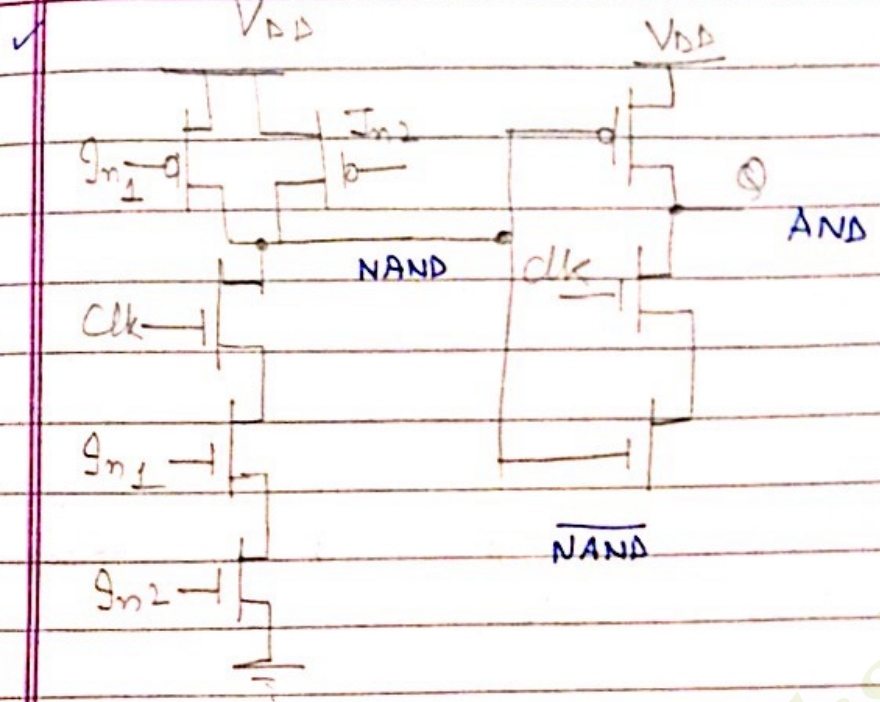
Clock pulses wasted
So, pipelining is done

Pipelining

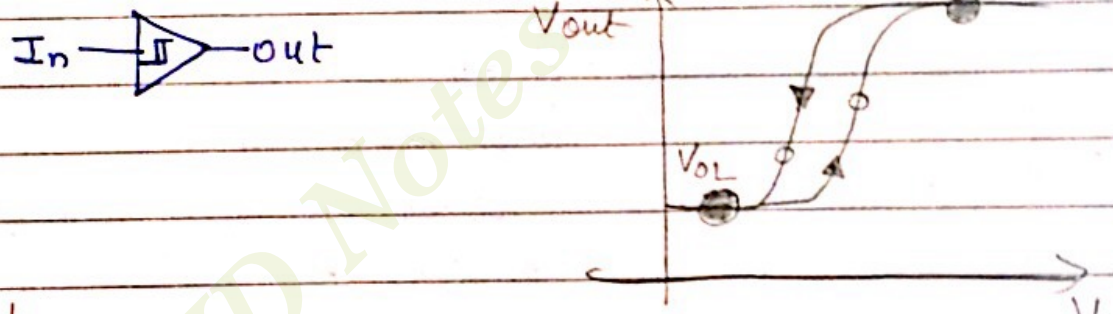


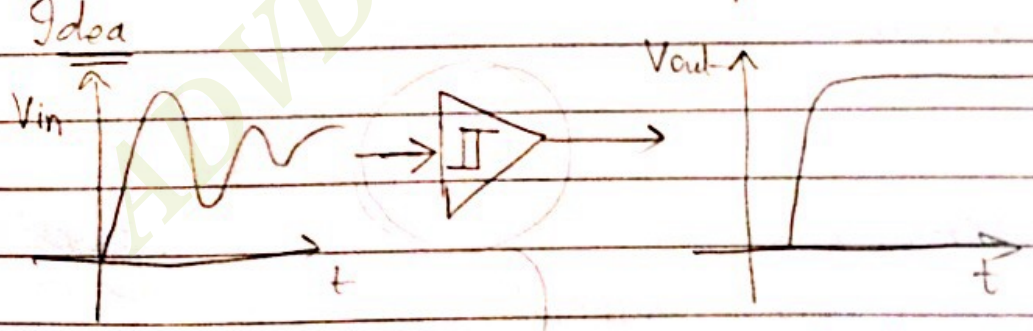
Clk period	fn ①	fn ②	fn ③	
1	f(x)			
2	f(y)	g(f(x))		
3	f(z)	g(f(y))	h(g(x))	Empty clock pulses used.
⋮	⋮	⋮	h(g(y))	
			⋮	

✱ Use of TSPC Latch to make AND.



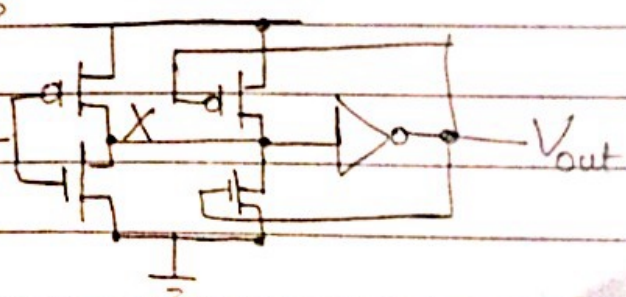
✱ Non Bistable Sequential Circuits: Schmitt Trigger





Time varying i/p — Constt o/p

Vin = D ↖ Vin = 1
X = 1 ; X = 0
Vout = $\bar{X}$ = 0 Vout = $\bar{X}$ = 1



• Schmitt Triggers are used to make FFs & VCO (Voltage Controlled Oscillators)

VLSI DESIGN CIRCUITS.

◦ Memory Defins :-

✓ Speed
- Read acess : delay b/w read request and data available.
- Write acess : delay b/w write request and writing of data into the memory.
- (Read or write) cycle : Min. time req^d b/w successive read or writes.

◦ Memories :

	Speed	Size	Cost
Secondary : external Hard disks.	less	(TB) More	Less
Main memory : DRAM.	↓	↓	↓
Second level cache : SRAM	more	(B) Less	More

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Date
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Read Write Memories (RWM)		NVRWM	ROM
Random Access	Non-Random access	EPROM	Mask. prog. ROM
SRAM (cache, register file)	FIFO, LIFO	EEPROM	
DRAM (main memory)	Shift register	FLASH	Electrically Prog. PROM
CAM			

SRAM	DRAM
• data is stored as long as power is supplied	• periodic refresh reqd (every 1-4 ms) to compensate for charge loss & due to leakage.
• large cells	• small cells.
• fast	• slow
• differential o/p	• single ended o/p
• compatible with CMOS	• Not compatible with CMOS.

* 3 diff memory architectures: 1D, 2D & 3D.

1D: N words, N select signals
(or) N words, select signals using decoder.

2D access of data: 2D addressing using Row & Column decoders.

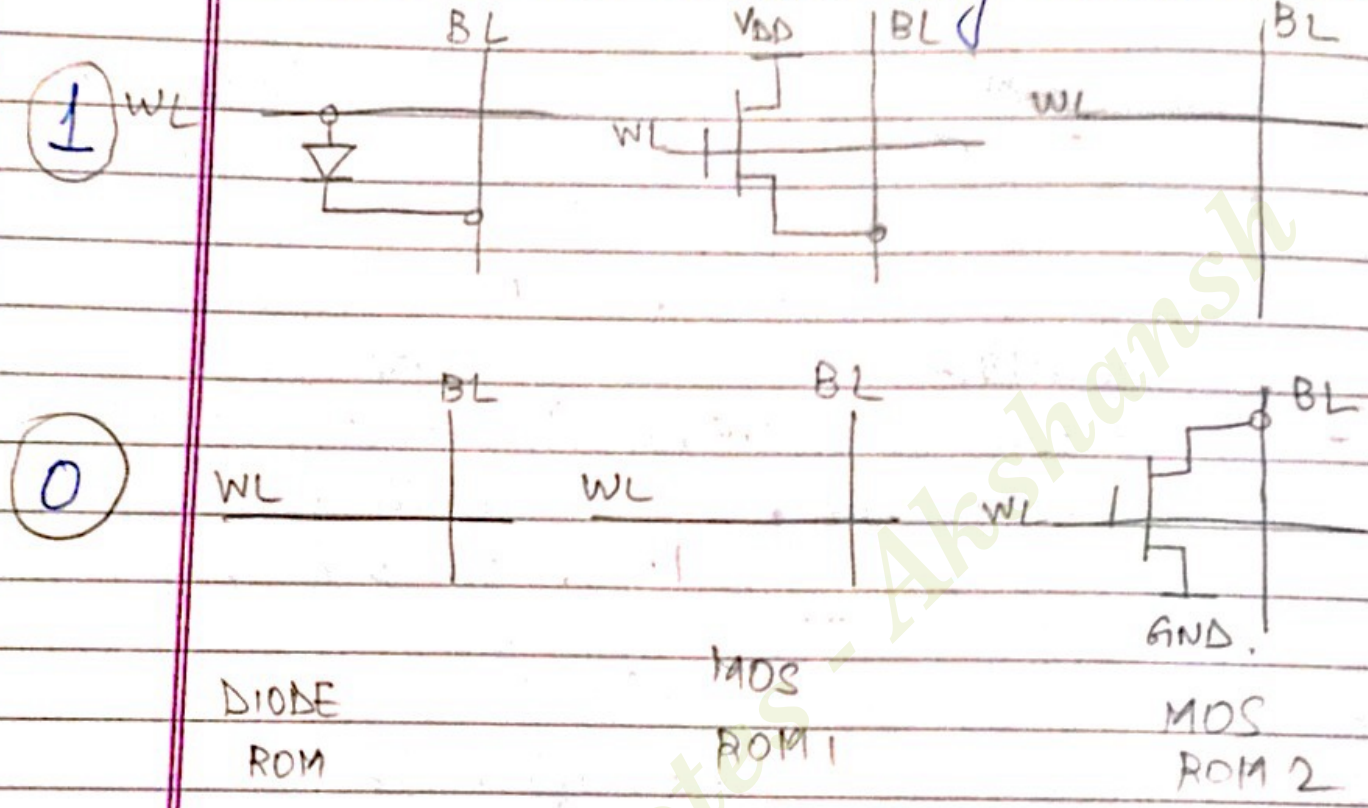
3D addressing: Row address + Col. address + Block address.

WL : Word line (≡ i/p)

BL : Bit line (≡ o/p)

Diagrams:- 6 transistors SRAM storage cell.

* ROM cells can be made using diodes or transistors.



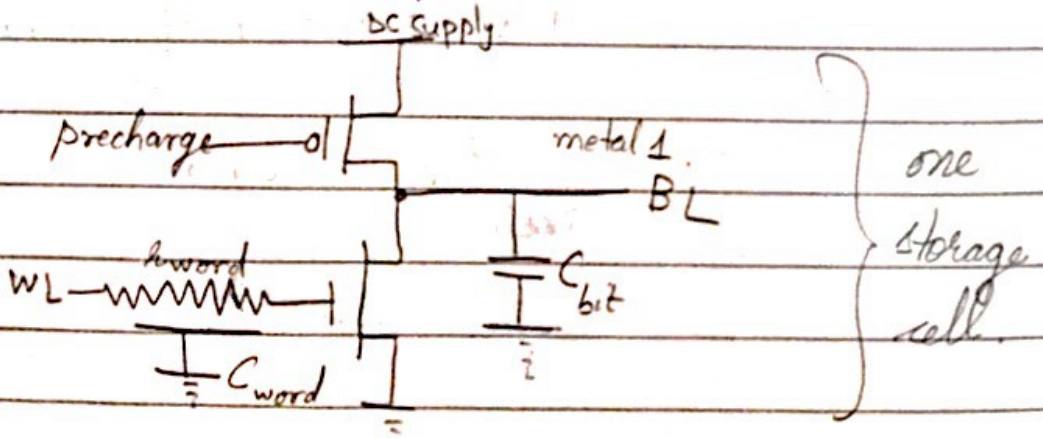
DIODE ROM

MOS ROM 1

MOS ROM 2

* Above is used in MOS ROM cell Arrays.
  - Implementing OR, NOR, NAND functions

° Transient model of 512x512 NOR ROM.



Word line Response time,

$$t_{word} = 0.38 (R_{word} \times C_{word}) \times M^2$$

(for one storage cell; M^2 for $M \times M$ NOR ROM)

If

Resistance/cell = 17.5 Ω

Wire capacitance/cell = 0.049 fF

Gate capacitance/cell = 0.75 fF

then,

$R_{word} = 17.5\ \Omega$, $C_{word} = 0.049 + 0.75$ fF

Bit line Response time,

$$C_{bit} = (M \times (0.09\ fF + 0.8\ fF) = 0.46\ pF$$

($M = 512$, here.)

$$t_{(HL)} = 0.69 \left(\frac{13\ k\Omega}{2} \parallel \left(\frac{31\ k\Omega}{5.25} \right) \right) \times C_{bit}$$

$t_{(HL)}$: high to low transn

$\left(\frac{W}{L}\right)_{NMOS}$ $\left(\frac{W}{L}\right)_{PMOS}$

$$\Rightarrow t_{HL} = 0.98\ ns.$$

$$t_{(LH)} = 0.69 \left(\frac{31\ k\Omega}{5.25} \right) \times 0.46\ pF$$

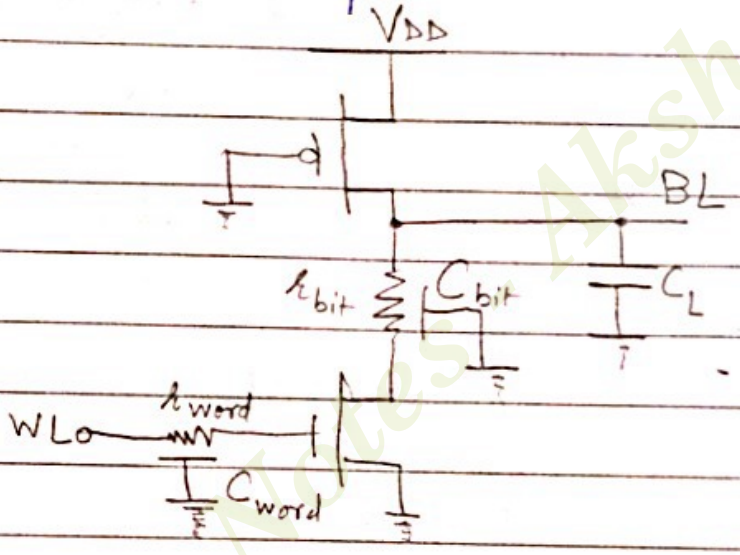
$t_{(LH)}$: low to high transn $= 1.87$ ns

* Static Power Dissipation
  - assuming 50% of o/p are low.
  - assuming standby current = 0.21 mA
    & o/p voltage = 15 V.

Total static dissipated power = $\frac{512}{2} \times 0.21\,mA \times 15$

$= 0.14\,W$

* Transient model for 512X512 MOS NAND ROM:

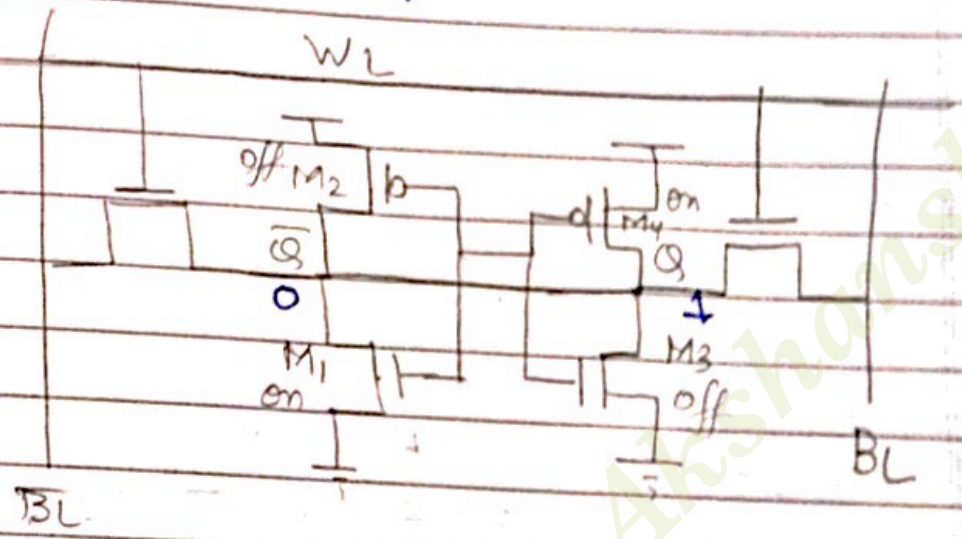


Details in slides and/or book

* SRAM cell analysis
  Changing voltage of BL & seeing noise
  Charging of capacitor is also shown.
* Multiple Read/Write Port Storage cell
* 3-transistor DRAM cell:
  ↳ 3 transistors remain. One of them is replaced by capacitor.
* 1-Transistor DRAM cell.
* 2D-4X4 RAM Memory
* Differential Sense Amplifier.

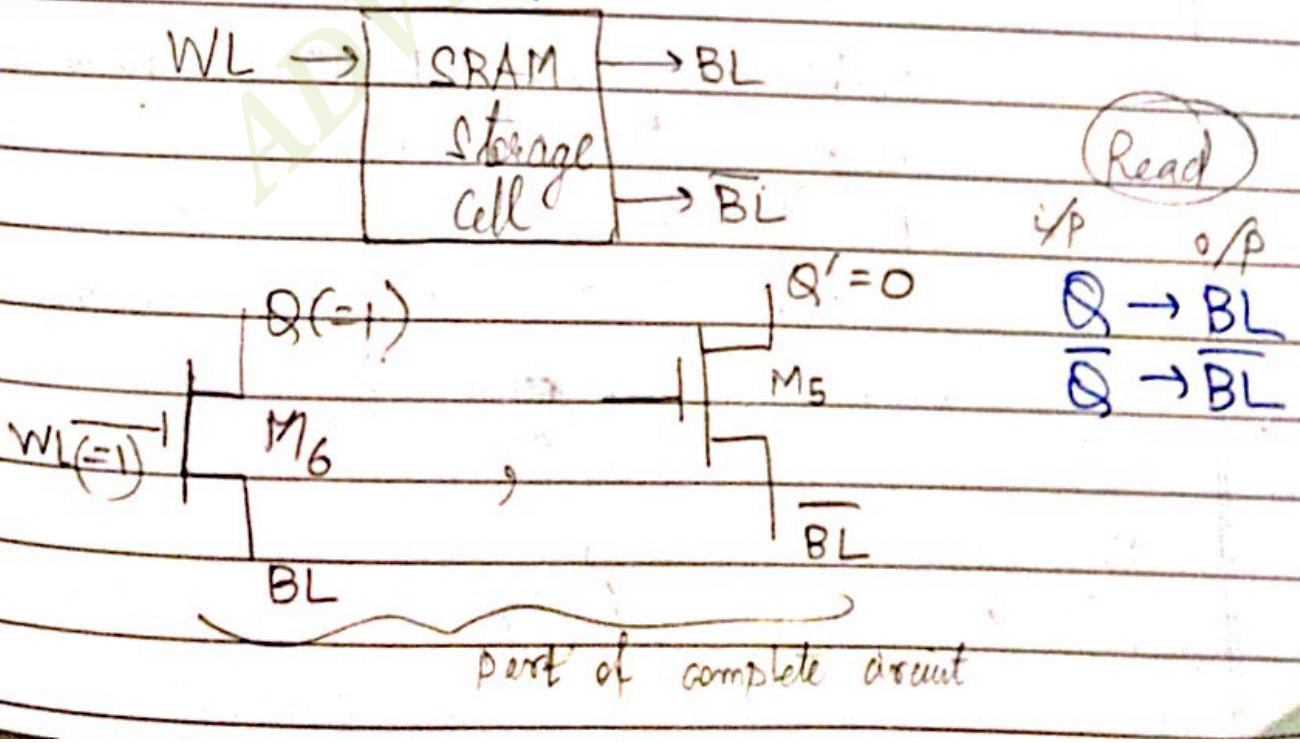
• Sense amplifier :-
Takes signal coming out of decoder.

Imp 6-transistor SRAM Storage Cell

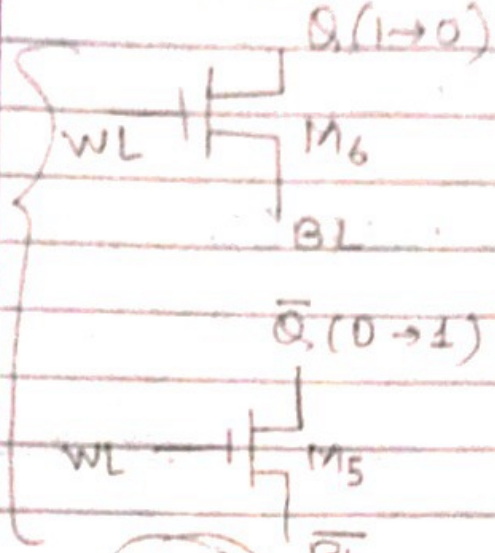


I'm seeing the state of my transistor. By changing the value of Q & Q̄ as 0 or 1, I see if the transistor is ON or OFF

SRAM cell analysis (Read)



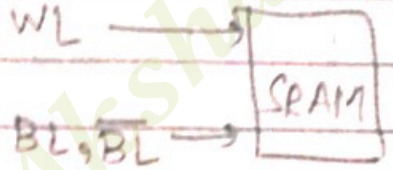
SRAM Write



When Q becomes from 1 to 0, data is discharged through the capacitor (from BL)

BL : Data/bit to be written.

Block diagram :



Write

i/p → o/p

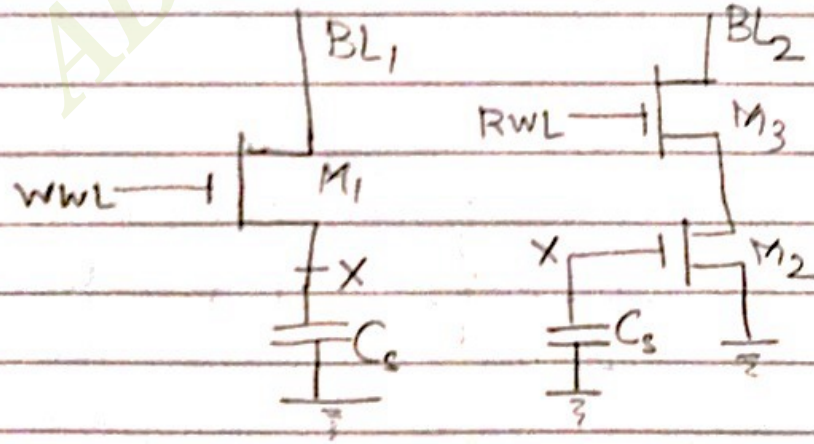
BL → Q

B̄L → Q̄

* Storing of info takes place in transistors (for SRAM)

✱ 3-Transistor DRAM cell :

∃ 2 separate Read & Write signals i.e, before we had WL. Now WWL & RWL



Write

Read

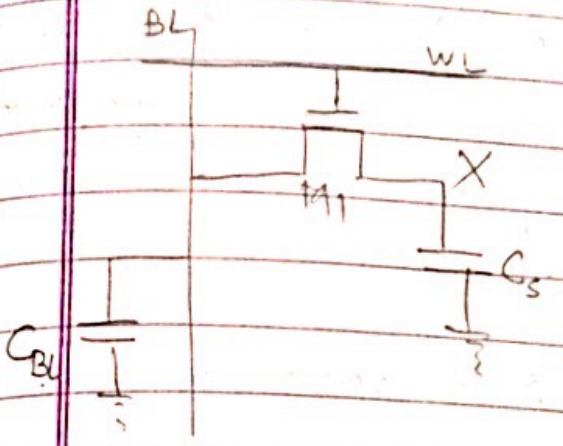
✱ ∃ 2 separate o/p lines for Read & Write (BL1 & BL2)

✱ Storing of info takes place in C_s. (for DRAM)

* Asserting WWL means make WWL = 1

* 1-transistor DRAM cell

(graph in Slides/book)



$X_1 = 1$ (C_S fully charged)

WL → 1 (Read)

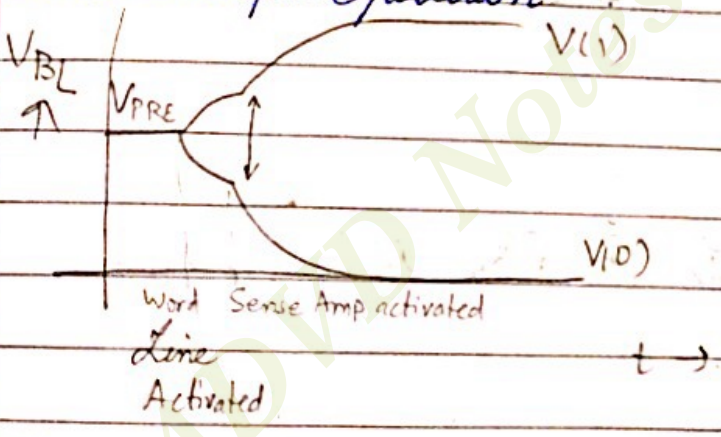
M_1 → SC

C_S discharges through C_{BL}

↳ X → 0.

(Requires REFRESH)

* Sense Amp. Operation



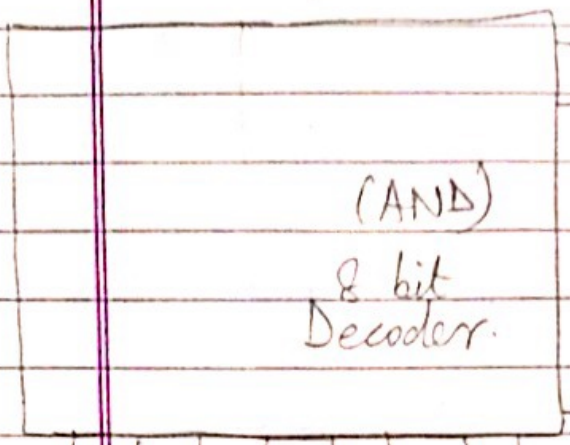
* 2D 4X4 RAM Memory:

* Row Decoders:

Collection of 2^M complex logic gates organized in a regular, dense fashion.

* In memory: read one bit at a time.

* NAND decoder for 8 bit address bits



$\overline{A_7}\,\overline{A_6}\,\overline{A_5}\,\overline{A_4}\,\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,\overline{A_0} \rightarrow WL(0)=1$, Rest $=0$

$\overline{A_7}\,\overline{A_6}\,\overline{A_5}\,\overline{A_4}\,\overline{A_3}\,\overline{A_2}\,A_1\,A_0 \rightarrow WL(1)=1$, Rest $=0$

$A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0 \rightarrow WL(255)=1$, Rest $=0$

$2^8 = 256$ outputs.

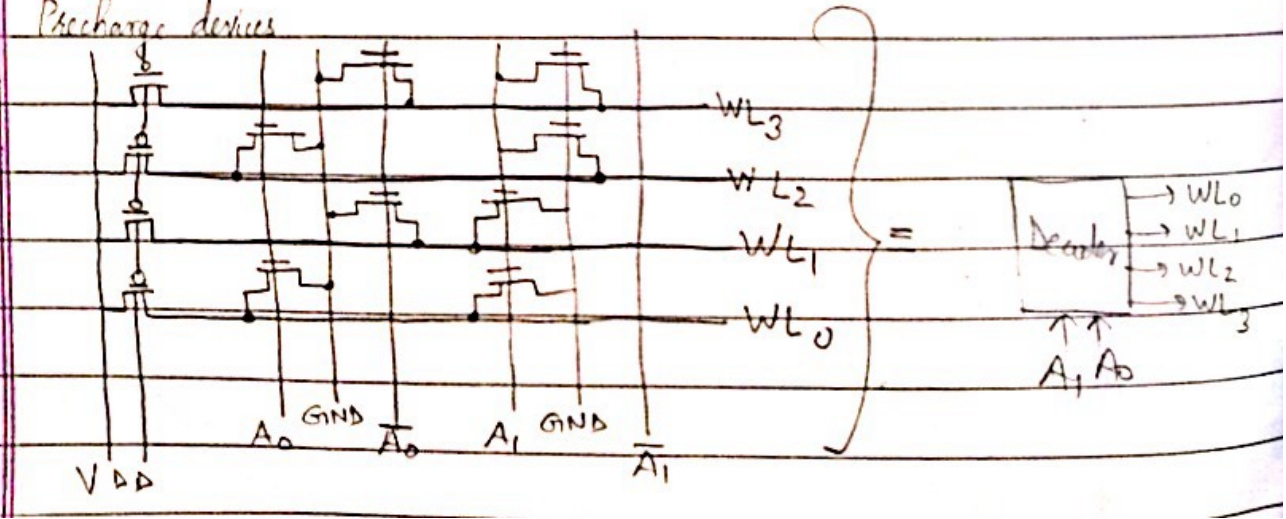
* NOR Decoder

8-bit, say

$WL(0) = \overline{A_7 + A_6 + A_5 + A_4 + A_3 + A_2 + A_1 + A_0}$

$WL(255) = \overline{\overline{A_7} + \overline{A_6} + \overline{A_5} + \overline{A_4} + \overline{A_3} + \overline{A_2} + \overline{A_1} + \overline{A_0}}$

* 2-input NOR decoder



A_1	A_0	WL_0	WL_1	WL_2	WL_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$WL_0 = \overline{A_1}\,\overline{A_0} = \overline{A_1 + A_0}$

$WL_1 = \overline{A_1}\,A_0 = \overline{A_1 + \overline{A_0}}$

$WL_2 = A_1\,\overline{A_0} = \overline{\overline{A_1} + A_0}$

$WL_3 = A_1 A_0 = \overline{\overline{A_1} + \overline{A_0}}$

* Differential Sense Amplifier
(directly applicable to SRAM.)

Date 18.12.13
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Ch: Introduction to Testing

→ deals with probability finding to analyse sales of any good, say.
→ use of Baye's Theorem & others are done.

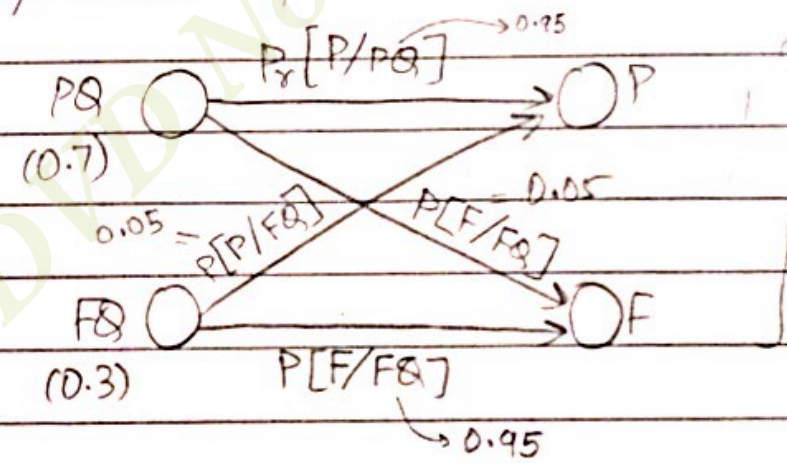
Example: (Showing diff probabilities & how they are used)

Assume: PQ: Student is pass quality
FQ: Student is fail quality.
P: Student passes test
F: Student fails test

Say, Prob (PQ) = 0.7 → Probability of P s.t. PQ is given
Prob (FQ) = 0.3

conditional probability → Prob [P/PQ] = 0.95 } * Total = 1
Prob [F/PQ] = 0.05

Seeing all possibilities of PQ → P, F & FQ → P, F



Sum as: probability of bits being transmitted.

from fig. $P_r[P] = \begin{cases} P[P/PQ] \times P[PQ] \\ + \\ P[P/FQ] \times P[FQ] \end{cases} = \begin{cases} (0.95)(0.7) \\ + \\ (0.05)(0.3) \end{cases}$

$\Rightarrow P_r[P] = 0.68$

& $P_r[F] = 1 - 0.68 = 0.32$

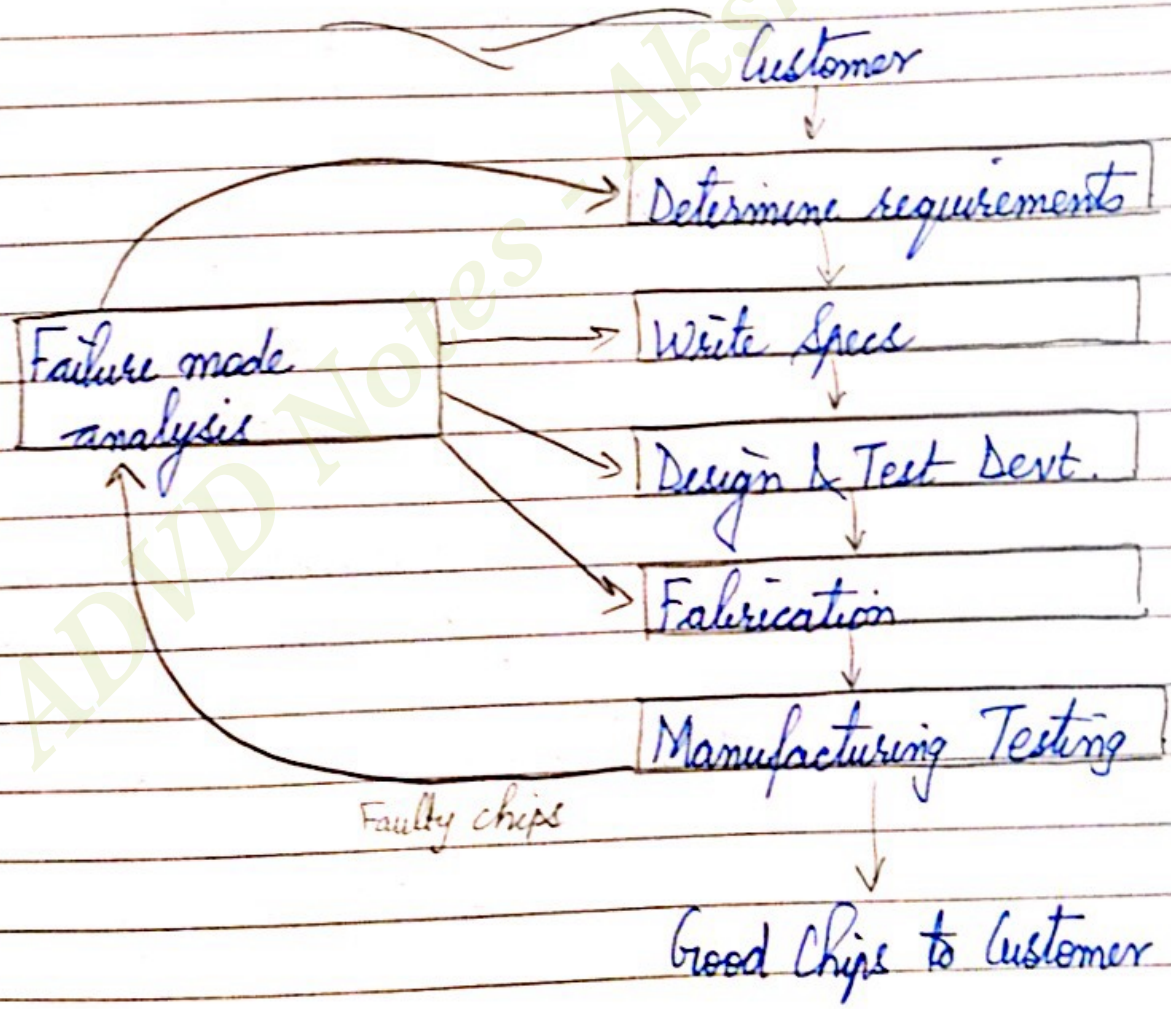
* FMA : Failure mode Analysis

Joint probability :

* $P_r[FQ, P] = P_r[FQ/P]\, P_r[P]$
$= P_r[P/FQ]\, P_r[FQ]$

* Bayes Rule / Theorem :

$$P_r[FQ/P] = \frac{P_r[F/FQ]\, P_r[FQ]}{P_r[P]}$$



* Note :
∃ Audit at every pt. of design manufacturing process

Fig : Given : manufacture sth for customer.
Idea : To : how to analyse every stage to prevent failure of any design / IC (i.e. its costly)

* For all the stages shown before, there are engineers at each stage (Field applic^n engineers, Testing engineer, Manufacturing engineer, VLSI design engineer, Systems engineer, Marketing & Sales engineer) which look into every detail to prevent failure.

* Testing in Purchase of product :

* Purchase Price is imp. factor for testing.

(ATE) • Purchase Price = $1.2 + 1024 × $3000
(# of pins, cost per pin)

= $4.272 M

• Running cost (per year) = Depreciation + Maintenance + Operating cost

20% of Purchase Price = (0.854M)

Maintenance → 2% (± 0.085M)

Operating cost → 0.5M (by historical data)

= $1.439 M/year

• Testing cost = Running cost / (365 × 24 × 3600) = 4.5 cents/sec.

↳ mostly, working is done in 3 shifts, 8 hours/shift

a way of designing IC.

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Eg. ASIC requires 6 sec of testing.

So,

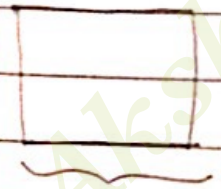
Cost = 4.5 × 6 = 27 cents

Suppose that only 65 % of the chips made worked

So. Test complement cost of one chip = $\frac{27}{0.65}$ = 41.5 cents

Now,

Assume a square chip : d



* No. of transistors that can be placed on chip, $N_t \propto d^2$
* No. of i/o pins that can be placed, $N_p \propto 4d$
* $N_p = k\sqrt{N_t}$
  - → from historical data
* Power Density = $C \times V_{DD}^2 \times f$
  - → Capacitance
  - → frequency
  - → Self : Read through constt. electric field scaling

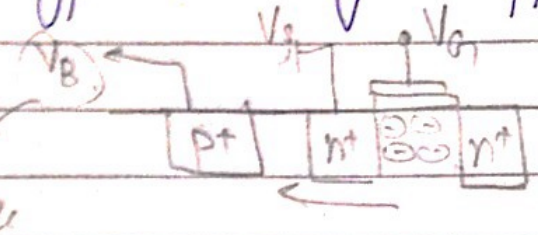
MOSFET converts V_G to I_D.

Credits: ece rack

ADVD Revision

2nd Order Effects:

- **Body Effect / Back gate effect**

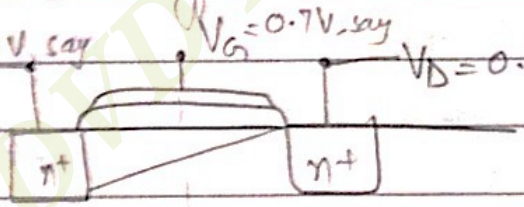


B/w gate & semiconductor, ∃ mirroring. i.e, as much potential at V_G is applied, so, no. of -ve charges are formed.

Thus, if $V_G = 0$, $V_B < V_S$, then V_B (base) will attract +ve charge from substrate so this will disturb mirroring, demanding extra requirement of V_G. So, ∵ $V_{th} \uparrow$, So, $V_{th} \uparrow$ (due to change in bulk voltage). This is called Body effect.

- **Channel length modulation:**

If V_S and V_D have different voltages, then $V_G - V_S$ is different than $V_G - V_D$.



$V_{GS} = 0.7V$

$V_{GD} = 0.2V$.

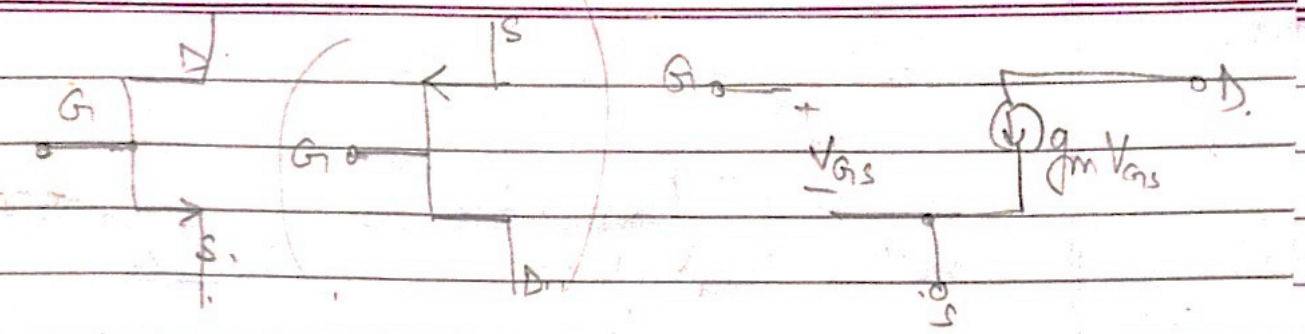
V_{GS} is more, so, channel is more in 1st half than second half ($V_{GD} < V_{GS}$) as shown. So, the change in channel width due to change in V_D is called Channel length modulation.

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

- **Sub-threshold Conduction:**

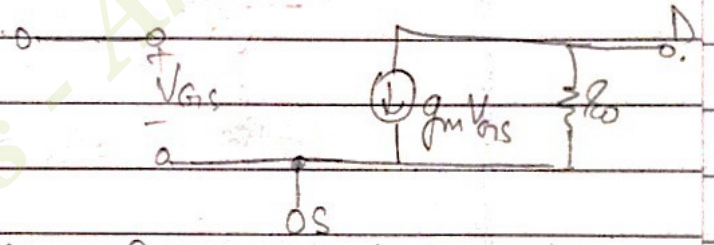
Sub-threshold is the time when $V_G < V_{th}$. So, although, there shouldn't be any conduction, some current is still there, $I_D = I_0 \exp \frac{V_{GS}}{\xi V_T}$, $\xi > 1$ (non ideality factor)

* Resistor ≡ Current source placed in voltage.



$$g_m = \frac{\delta I_D}{\delta V_{GS}}.$$

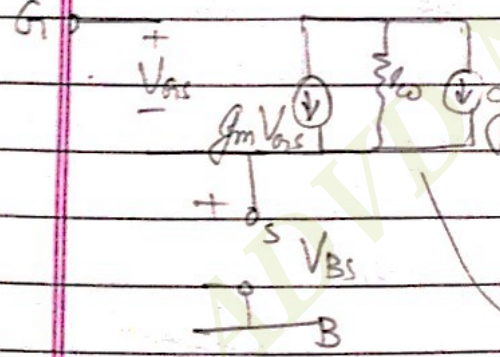
* In channel length modul^n, ∃ changes in current value. So, ∵ current is changing, so we can put a current source (r_o or resistance) in parallel to $g_m V_{GS}$.



$$r_o = \frac{\delta V_{DS}}{\delta I_D} = \frac{1}{\frac{\delta I_D}{\delta V_{DS}}} \rightarrow \text{from eqn.}$$

$$\therefore \boxed{r_o = \frac{1}{\lambda I_D}}$$

* In body effect, ∃ voltage diff b/w source & bulk. So, ∃ additional current term in circuit.



Includes both Channel length modul^n & body effect

* Transconductance (g_m): It is the efficiency of MOSFET i.e., how much current will I get if I give some value of voltage i.e., $g_m = \left(\frac{\delta I_D}{\delta V_{GS}}\right)_{V_{DS} = \text{const}}$

→ Analog electronics, so, change (δ)

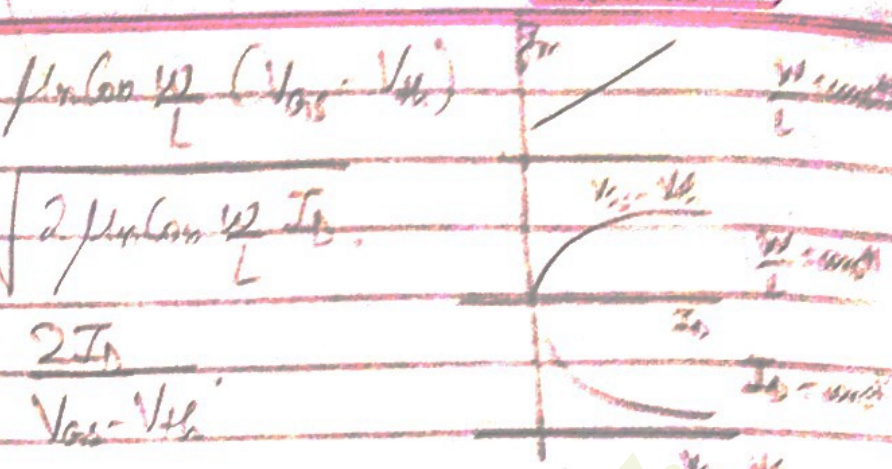
↑ comes on doing $\frac{\delta I_D}{\delta V_{GS}}$

Bullish
Buy

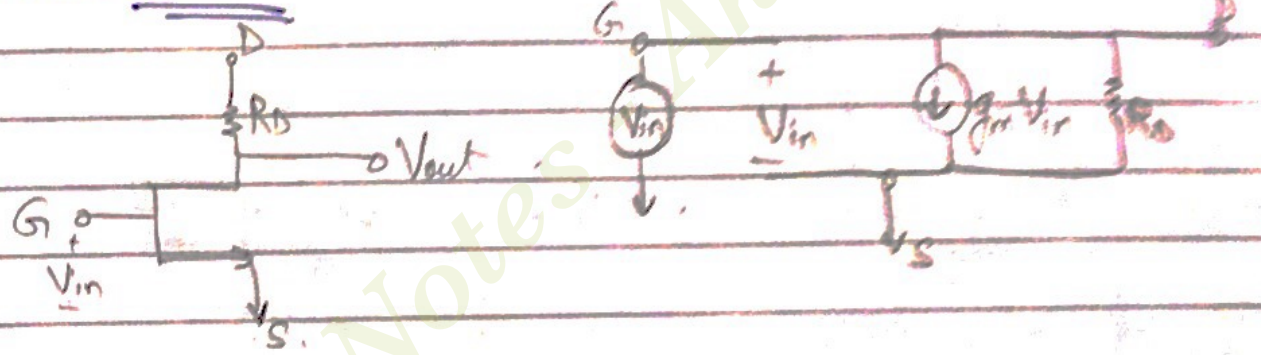
form of $g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})$

$= \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D}$

$= \frac{2 I_D}{V_{GS} - V_{th}}$



AMPLIFIERS



- Transistor in satur^n region : amplifier
  not in satur^n region : switch

Voltage gain = $A_V = \frac{\delta V_{out}}{\delta V_{in}}$

↳ For CS Amp, $V_{DS} = V_{DD} - I_D R_D$

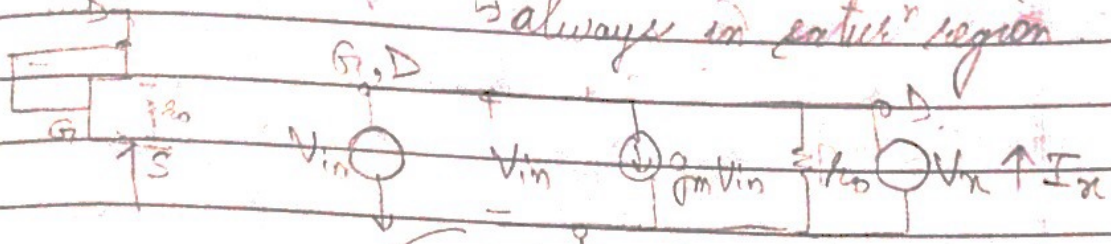
$\Rightarrow V_{out} = V_{DD} - \left(\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th})^2\right) R_D$

$\Rightarrow \frac{\delta V_{out}}{\delta V_{in}} = -g_m R_D$.

↳ So, a CS Amp. circuit amplifies if it has high efficiency (g_m) & low resistance

✱ Diode Connected Transistor

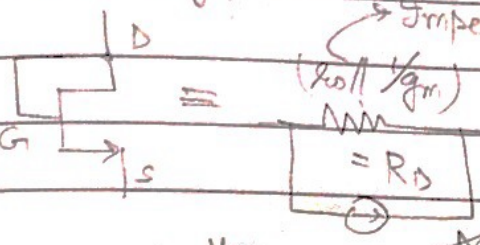
↳ always in saturation region



$V_{in} = V_x$

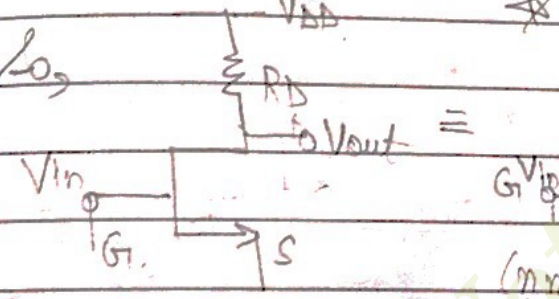
Impedance = $\frac{V_x}{I_x}$ of network $= R_x$

So, I can say

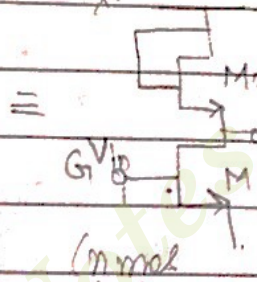


$\Rightarrow I_x = \frac{V_x}{r_o} + g_m V_x$

$\Rightarrow R_x = \frac{1}{g_m + 1/r_o} = r_o \,||\, 1/g_m$



$\equiv$



(mos diode connected)

$A_v = -g_{m1}(r_{o2} \,||\, 1/g_{m2})$

$\hookrightarrow r_{o2} \gg 1/g_{m2}$

$\Rightarrow A_v = -\frac{g_{m1}}{g_{m2}} \equiv -\frac{g_{m1}}{g_{m2} + g_{mb2}}$ (including body effect)

$\Rightarrow A_v = -\frac{g_{m1}}{g_{m2}\left(1 + \frac{g_{mb2}}{g_{m2}}\right)}$

$= -\frac{g_{m1}}{g_{m2}(1+\eta)}$ $\rightarrow \frac{g_{mb2}}{g_{m2}}$

$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D}$

$\Rightarrow I_{D1} = I_{D2}$ (current stays same.)

$\Rightarrow A_v = -\sqrt{\frac{2 \mu_n C_{ox} \frac{W_1}{L_1} I_{D1}}{2 \mu_n C_{ox} \frac{W_2}{L_2} I_{D2} (1+\eta)}} = -\frac{\sqrt{(W/L)_1} \times 1}{\sqrt{(W/L)_2}(1+\eta)}$

Gain of amplifier is independent of bias currents, voltages

★ For ckt to be in saturation

$V_{DS} \geq V_{GS} - V_{th}$

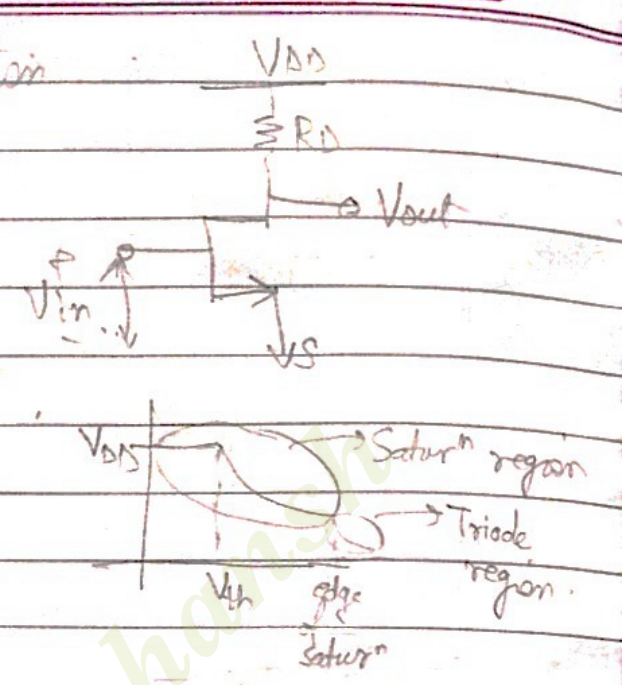
or $V_{out} \geq V_{in} - V_{th}$

& $V_{out} = V_{DD} - I_D R_D$

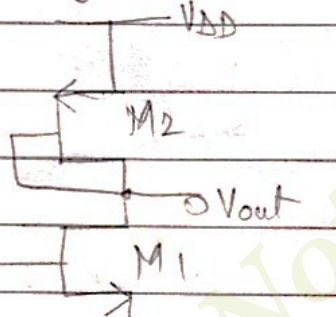
So,

$V_{in} \uparrow \Rightarrow I_D \uparrow \Rightarrow V_{out} \downarrow$.

So, at some point, satur^n goes



★ Using pmos diode connected transistor:



Ignoring body effect

$\mu_n = 2\mu_p$

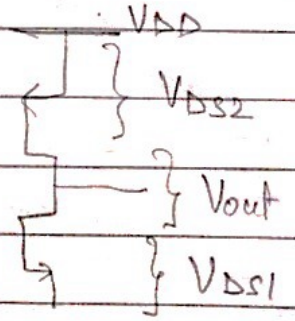
$A_V = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$

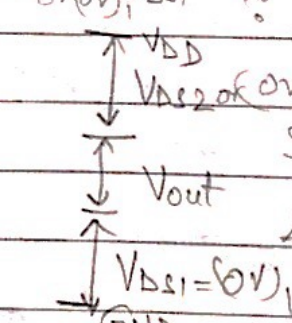
$\Rightarrow$ for a gain of 100, say, the size $\frac{(W/L)_1}{(W/L)_2} = 50$. So, M1 is 50 times larger than M2.

Now $I_{D2} = I_x$.

$\Rightarrow A_V = \frac{|V_{GS2} - V_{th2}|}{(V_{GS1} - V_{th1})}$ → V_{DS2} or $(OV)_2$

$\Rightarrow$ or $(OV)_1$ V_{DS1}

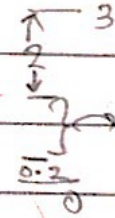




$\therefore$ for a gain of 10, $\frac{V_{DS2}}{V_{DS1}} = 10$

Say $V_{DD} = 3V$, $V_{DS1} = 900\,mV$

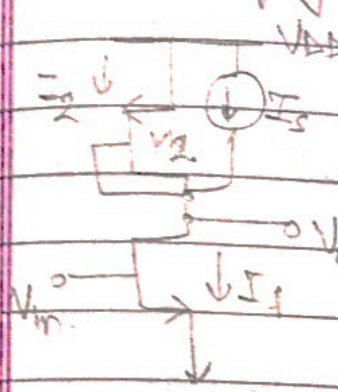
So, $V_{DS2} = 2V$. So,



So, Vout has a very low o/p swing

$V_{PP} = 0.8\,V$ So, not nicely detectable.

Now, changing transistor as:



$I_1 = I_2$

or $I_1 = \underbrace{0.25 I_1}_{I_2} + \underbrace{0.75 I_1}_{I_3}$ dividing I_2 into 2 parts

$\Rightarrow I_1 = \underbrace{\frac{I_1}{4}}_{I_2} + \underbrace{\frac{3}{4} I_1}_{I_3}$ (0.25 I_1 + 0.75 I_1 = I_1)

Now we have

$$A_v = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{2\mu_n C_{ox}(W/L)_1 I_{D1}}{2\mu_p C_{ox}(W/L)_2 I_{D2}}}$$

$$\Rightarrow A_v = -2\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} \quad \text{or} \quad \frac{A_v}{2} = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

Now, $I_{D1} = 4 I_{D2}$

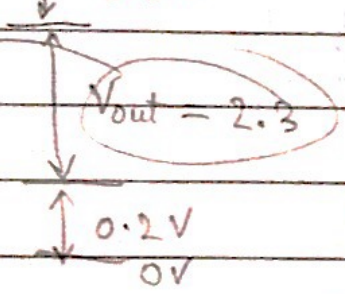
$$\Rightarrow \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS_1} - V_{th_1})^2 = \left(\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS_2} - V_{th_2})^2\right) 4$$

$$\Rightarrow \sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} = \left(\frac{|V_{GS_2} - V_{th_2}|}{(V_{GS_1} - V_{th_1})}\right) 2$$

$$\Rightarrow \frac{A_v}{4} = \frac{|V_{GS_2} - V_{th_2}|}{(V_{GS_1} - V_{th_1})} \quad \text{So, } \frac{A_v}{4} = \frac{(OV)_2}{(OV)_1} \text{ or } \frac{V_{DS2}}{V_{DS_1}}$$

So, Suppose again $V_{DD} = 3V$, $A_v = 10$, $(OV)_1 = 200mV$ c

$\Rightarrow (OV)_2 = 500\,mV$. So,

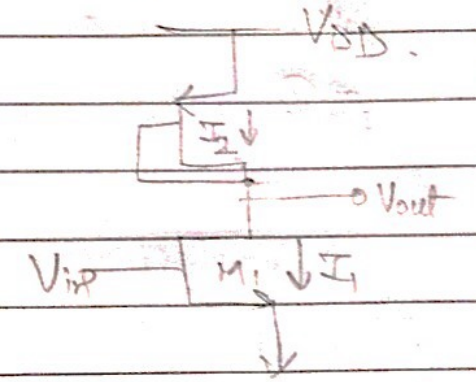


So, o/p voltage swing improved using current source.

* Note : A MOSFET in
triode region : behaves as a resistor.
saturation region : behaves as a resistor in parallel to a current source

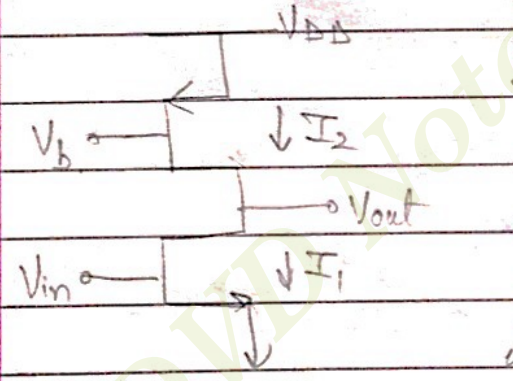
from MOSFET's I-V Char.

Previously, we made

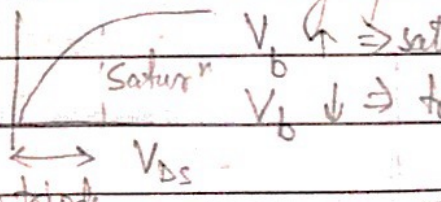


i.e., we used a diode connected load, which behaved as a resistor, in parallel to current source. But, we want only some replacement of resistor.

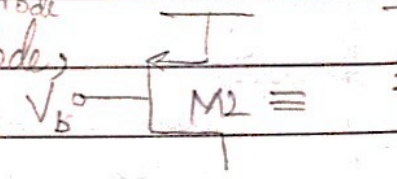
So, now, we are trying to make a MOSFET, in triode region.



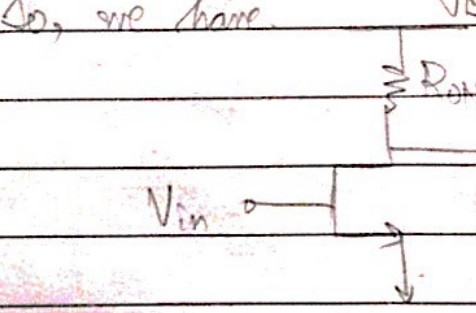
Idea : Include BIAS voltage, V_b instead of making it diode connected load. Now, since its a mosfet (we are changing a voltage in it



So, when biased, to behave in triode,



So, we have



$(g_m) = \mu_p C_{ox} \left(\frac{W}{L}\right)_2 \left(V_{SG} - |V_{th_p}|\right)$

for M2

here, $g_m = \frac{1}{R_{ON}}$

Way to remember: In satur° region (conducts) → so, see it as transCONDUCTANCE (g_m)

In triode region: (resistor). So, see it as $\frac{1}{R}$ (Resistance)

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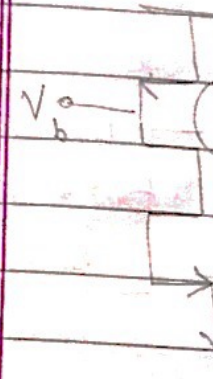
$$R_{ON_2} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS} - |V_{thp}|)}$$

$$= \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_S - V_G - |V_{thp}|)}$$



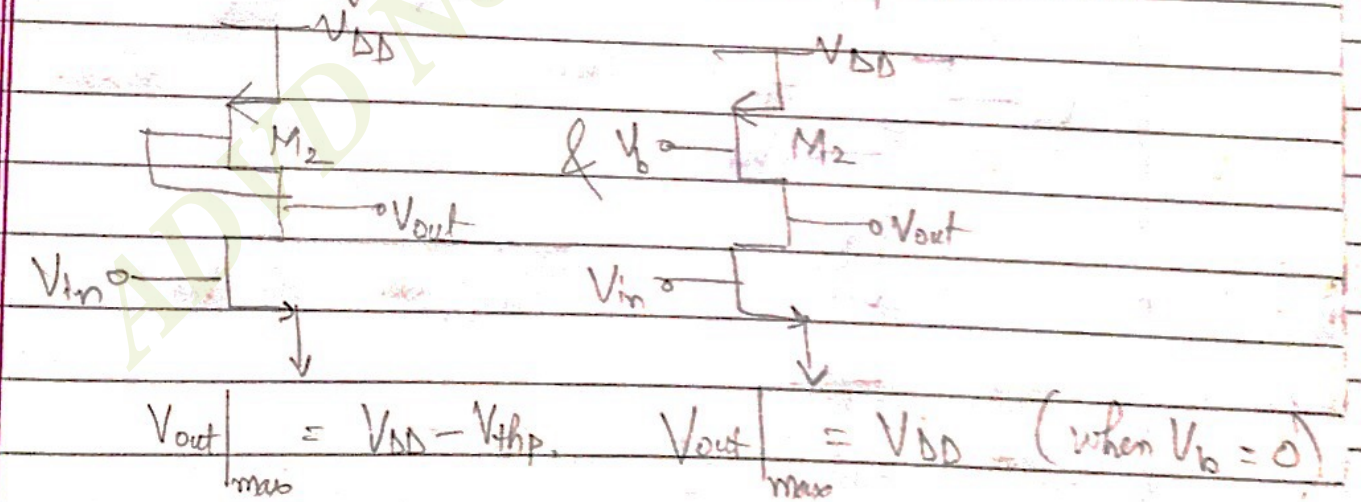
for M_2, $V_S = V_{DD}$, $V_G = V_b$

$$\Rightarrow R_{ON_2} = \frac{1}{\mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{DD} - V_b - |V_{thp}|)}$$

→ This resistance will replace my R_D (another way)

→ It has many terms that we have to look into, so, we don't use it

Now, seeing comparison b/w 2 of our circuits:



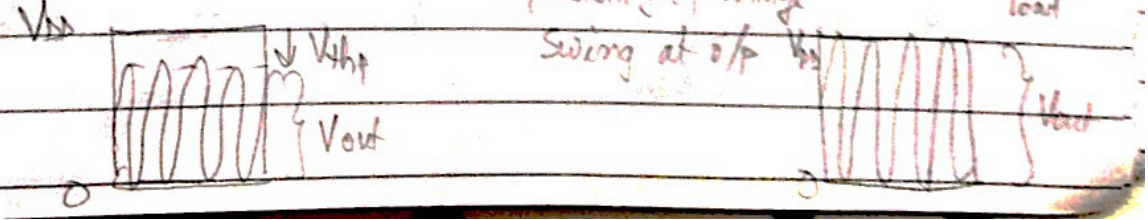
$V_{out}|_{max} = V_{DD} - V_{thp}$.

$V_{out}|_{max} = V_{DD}$ (when $V_b = 0$)

So, M_2 | as bias voltage has greater headroom than M_2 | diode connected load

possibility of voltage swing at o/p

i.e.,



* Driving a load ⇒ passing current through a resistor connected to load.

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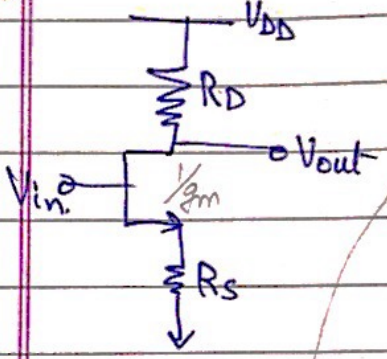
* CS Amp. with source degeneration : i.e including R_S



$$A_V = -\left(\frac{g_m}{1+g_m R_S}\right) R_D$$

↳ here, unlike previous gain $= -g_m R_D$, gain has reduced.

Taking $R_S \gg 1/g_m$, we get

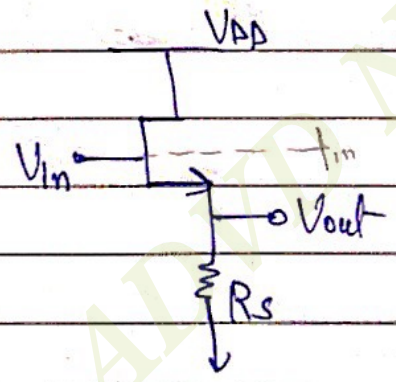
$$A_V = -\frac{1}{R_S} R_D \rightarrow \text{linearity}$$

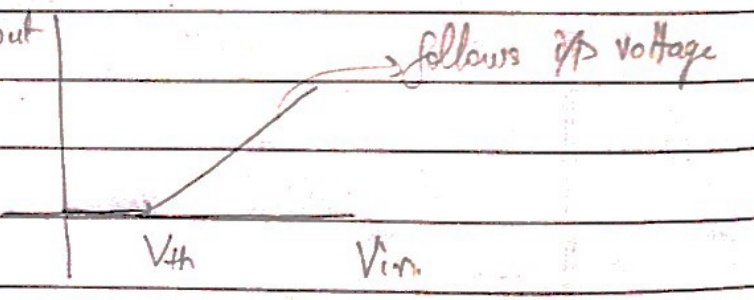
(But ↓ gain sacrificed)

$$A_V = -\frac{R_D}{(1/g_m + R_S)} \equiv -\frac{\text{Resistance in Drain path}}{\text{Resistance in Source path}}$$

* Common Drain Amplifier

↳ Called Source follower or Voltage Buffer or Buffer Stage.





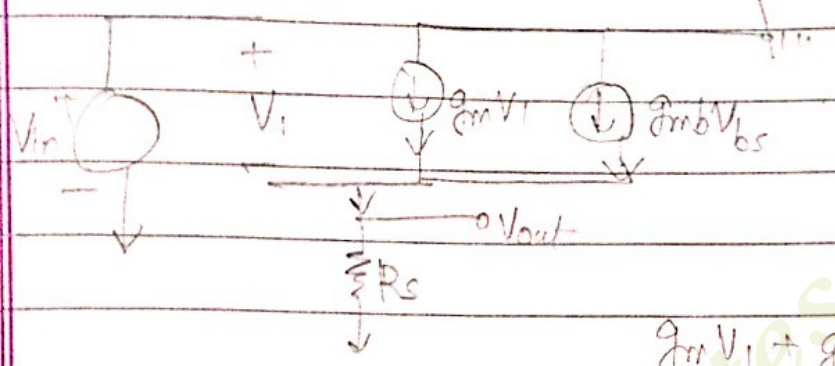
$$V_{out} = I R_S$$

$$\Rightarrow V_{out} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2 R_S$$

$$\Rightarrow V_{out} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{out} - V_{th})^2 R_S$$

$$\Rightarrow A_V = \frac{\delta V_{out}}{\delta V_{in}} = \frac{g_m R_S}{1 + R_S(g_m + g_{mb})}$$

Small signal model.



$V_{in} = V_1 + V_{out}$

$V_{bs} = V_b - V_s$

$= 0 - V_{out}$

$\Rightarrow V_{bs} = -V_{out}$

$$g_m V_1 + g_{mb} V_{bs} = \frac{V_{out}}{R_s}$$

$$\Rightarrow g_m (V_{in} - V_{out}) + g_{mb}(-V_{out})$$

$$\Rightarrow g_m V_{in} - V_{out}(g_m + g_{mb}) = \frac{V_{out}}{R_s} \qquad = \frac{V_{out}}{R_s}$$

Akshansh Chaudhary
2011AAPS300U

Reading Assignment
ADVD

Summary - Chapter-17 (Razavi)
CMOS Processing Technology.

In this chapter, we are mainly concerned with designing of a CMOS.

CMOS devices are primarily meant for digital applications, but, with some change in design and fabrication, they can be used in analog applications.

Now, Designing of CMOS: It has mainly three types of devices — Active devices, Passive Devices and Interconnect. The design varies with each of the device.

① Designing of Active Device:
It has 2 parts: Fabrication of transistor and introducing electrical connections in it.

For Fabrication, we need
- ✓ a base, on which transistor will be made
- ✓ a selector, for selecting areas of the base
- ✓ a protector, for protecting the layers created
- ✓ a generator, for making n-type & p-type regions
- ✓ a depositor, for putting/depositing required materials one-by-one.
- ✓ a destroyer, which removes unwanted material/regions during fabrication.

The processes involved in these are:

✓ Base : Wafer Processing
✓ Selector : Photolithography
✓ Protector : Oxidation
✓ Generator : Ion Implantation .
✓ Depositor : Deposition .
✓ Destroyer : Etching

With these processes and tools used appropriately, a transistor is fabricated.

Now, introduction of electrical connections is done.
The idea is to reduce the high resistance of the newly fabricated transistor and then putting Aluminium or copper (thin) layers over it (along with protection done side by side). The reduction, (initial step) is done ~~is done~~ in resistance by 'Silicidation'.

Around 5 layers of metals & 10 masks for it are created to finish making the active device.

② Designing of Passive Devices:

This includes designing of Resistors and Capacitors.

Now, while introducing electrical connections, silicide layer was put over the polysilicon to reduce its resistance. Hence, blocking the silicide layer deposition by using an appropriate mask (via lithography) makes it a Resistance.

Now, for designing a capacitor, idea is to make two conductors and a dielectric between them. So, we take these conductors as are metal and/or polysilicon, and the dielectric as thin oxide layer between them.

Note: We saw that, say, for an NMOS, giving +ve charge to gate induces -ve charge and hence creates an inversion layer (on p-substrate) (for making conduction possible); this behaviour is also like a capacitor. So, in CMOS, capacitance is seen even between a polysilicon layer and ~~diffusion~~ n-type or p-type substrate.

③ Designing of Interconnect:

This basically includes how will the metal layers be connected and what will be the layer width.

The idea is to reduce transmission losses over long distances.

So, for this, the width of the layer is varied depending upon whether the metal layer is in upper level or lower level of transistor.

* Latch-up:

This is a phenomenon seen in CMOS devices when the loop gain is greater than or equal to unity. In this case, the transistors draw enormous current from V_{DD}. It is a drawback of using CMOS and needs to be monitored by choosing appropriate value of loop gain.