MICROELECTRONIC CIRCUITS NOTES

AKSHANSH CHAUDHARY

Microelectronic Circuits Notes, First Edition

Copyright © 2013 Akshansh

ALL RIGHTS RESERVED.

Presented by: Akshansh Chaudhary
Graduate of BITS Pilani, Dubai Campus
Batch of 2011

Course content by: Dr. Jagadish Nayak
Then Faculty, BITS Pilani, Dubai Campus

Layout design by: AC Creations © 2013



The course content was prepared during Spring, 2013.
More content available at: www.Akshansh.weebly.com

DISCLAIMER: While the document has attempted to make the information as accurate as possible, the information on this document is for personal and/or educational use only and is provided in good faith without any express or implied warranty. There is no guarantee given as to the accuracy or currency of any individual items. The document does not accept responsibility for any loss or damage occasioned by use of the information contained and acknowledges credit of author(s) where ever due. While the document makes every effort to ensure the availability and integrity of its resources, it cannot guarantee that these will always be available, and/or free of any defects, including viruses. Users should take this into account when accessing the resources. All access and use is at the risk of the user and owner reserves that right to control or deny access.
Information, notes, models, graph etc. provided about subjects, topics, units, courses and any other similar arrangements for course/paper, are an expression to facilitate ease of learning and dissemination of views/personal understanding and as such they are not to be taken as a firm offer or undertaking. The document reserves the right to discontinue or vary such subjects, topic, units, courses, or arrangements at any time without notice and to impose limitations on accessibility in any course.

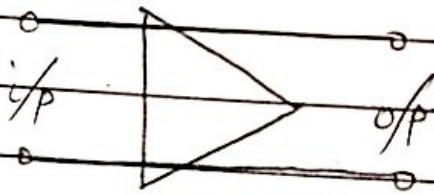
Puffin
Date 5.2.13
Page

Introduction to Amplifiers

* Amplifier : ✓ System
  ✓ Enhances signal
  ✓ no change in shape of signal.

* Amplifying a signal.

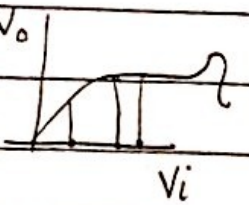
• Differential ended i/p & differential ended o/p.



$V_o(t) = A V_i(t)$ (A: Amplific" factor or Amplifier's gain; V_o: o/p voltage; V_i: i/p voltage)

• Faithful reproduction of signal :-
  ⇒ Shape f^n of i/p = Shape f^n of o/p
  eg. (Sinusoidal wave)$_{i/p}$ = (Sinusoidal wave)$_{o/p}$.
  → Possible when ∃ linearity.

* In case of non linearity → eg.



eg : $V_o = A(V_i)^2$

• In daily life, we mostly have non linear signals. So to use linear signals, take only the part that is linear. That part is small. So, oper^n is done at low voltage for making linear.

Microelectronic Circuits Nitin Akshansh

Instl : Instantaneous

- Voltage amplifier : amplifies voltage signals (less or no current amplification)
- Current amplifier : amplifies current signals (can amplify voltage also, but we don't use it like that)
- Voltage gain, $A_v = \frac{V_o}{V_i} = A_V$

  (in dB, it is $20 \log |A_v|$ dB)
- eg. voltage gain = 1000.

  $\Rightarrow 20 \log |1000| = 60$ dB
- Current gain, $A_i = \frac{I_o}{i_i}$

  (in dB, it is $20 \log |A_i|$ dB)
- Power Gain, $A_p = \frac{P_L}{P_i} \left(\frac{V_o I_o}{V_i I_i}\right)$ (Load power / i/p Power)

  (in dB, it is $10 \log |A_p|$ dB)

$A_v \cdot A_i$

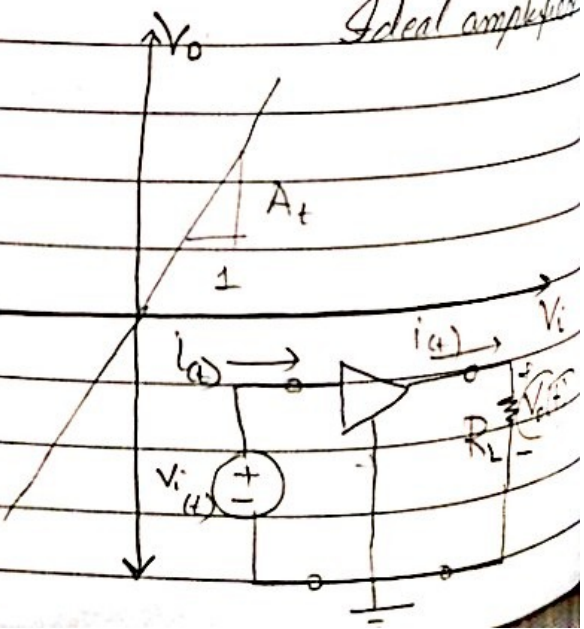
P_L / P_i

$\rightarrow (V_o)_{rms} \cdot (I_o)_{rms}$

$= \frac{V_o}{\sqrt{2}} \cdot \frac{I_o}{\sqrt{2}}$ → Peak Values.

$\rightarrow (V_i)_{rms} \cdot (I_i)_{rms}$

$= \frac{V_i}{\sqrt{2}} \cdot \frac{I_i}{\sqrt{2}}$

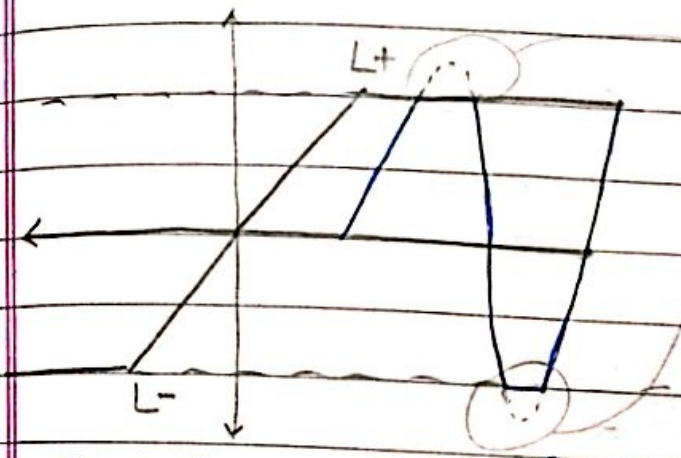


Microelectronic Circuits Notes, Akshansh

In a practical amplifier, ∃ limits → L+ & L− ∵ satur" region

• Output Satur" Effect :-

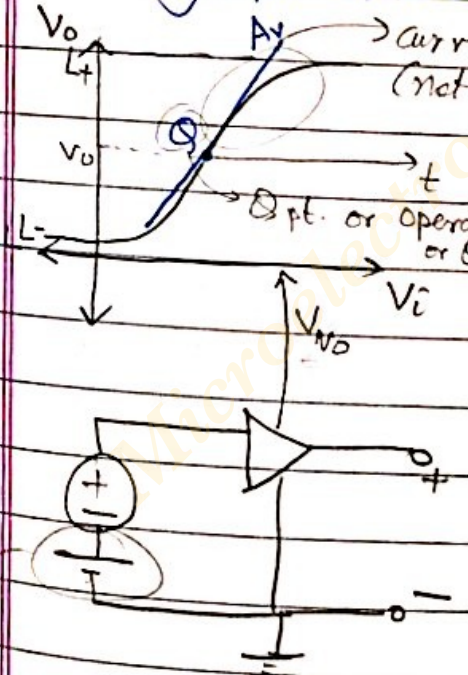
To ensure linear oper", i/p signal must be kept within linear range of oper".



get clipped off. if signal > L+ or < L−.

§ NON Linear Transfer Char. & BIASING

• In reality, a sharp edge transfer characteristics don't occur. Plus, alongwith AC (our signals transmitted by us), ∃ DC supply also (sth like battery to make the ~~circuit~~ transmission work)



Moreover, an amplifier amplifying the signal will also need DC supply to energize itself.

Inside internal circuit, to implement this, a biasing technique is applied.

S1) Apply DC voltage VI

S2) Instt. i/p $V_I(t) = V_I + V_i(t)$

S3) Correspondingly,

$V_O(t) = V_o + V_o(t)$

S4) Note :- A_V is slope of linear segment at Q.

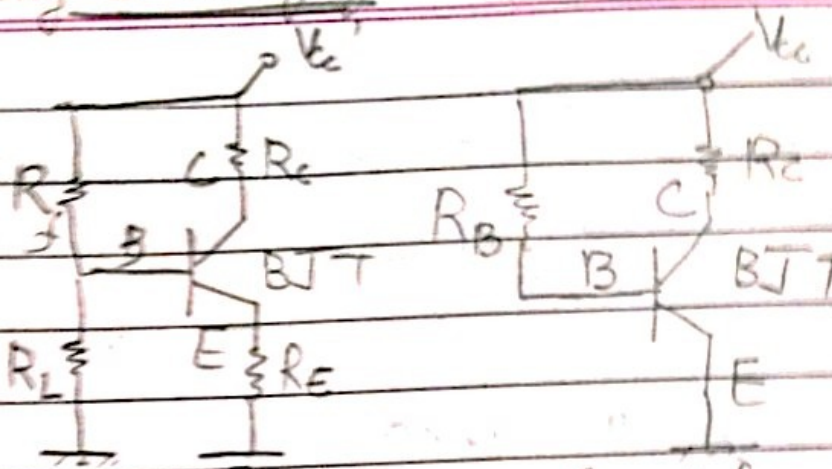
$A_V = \text{slope} = \frac{\Delta y}{\Delta x} = \frac{V_o(t)}{V_i(t)}$ → S4) $V_o(t) = A_V V_i(t)$

Q pt. :- Pt. on transfer char. where device is operating

Anurag Electronics Circuit Notes_Akshansh

* Ignore anything if its $\frac{1}{10}^{th}$ or less

Way to energize



Self bias ckt fixed bias ckt

* Amplifier Power Supplies

✓ DC power delivered to amplifier $P_{dc} = V_1 I_1 + V_2 I_2$

✓ From circuit (see book)

$$P_{dc} + P_I = P_L + P_{dissipated}$$

P_I → very less, so, ignored

✓ Performance factor; efficiency, $\eta = \frac{P_L \times 100}{P_{dc}}$

✓ Note :- In a transformer o/p P = i/p Power
In an amplifier o/p P > i/p P

✓ Power dissipated within device appears as heat.

Self * See for Symbol Conventions →

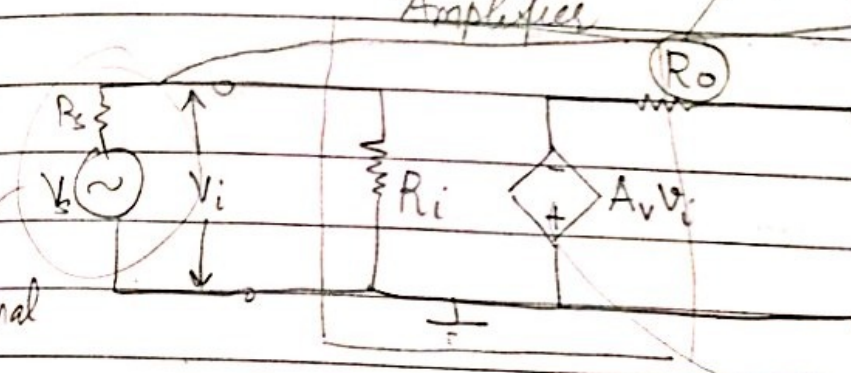
Equivalent ckt :- Voltage source → Replace by a short circuit | Current Source → Replace by OC

Puffin
Date
Page

AMPLIFIERS : Circuit Model

Making a circuit for practical purpose.

Amplifier



By potential divider rule,

$V_i = \left(\frac{R_i}{R_i + R_s}\right) V_s$

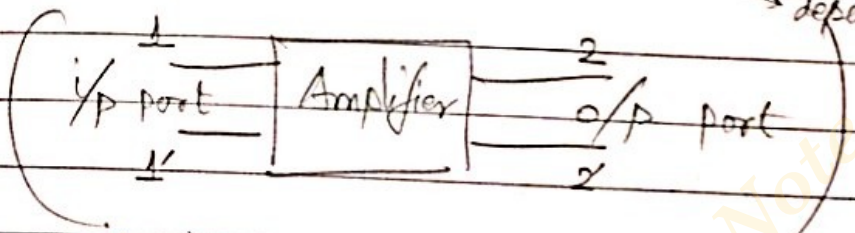
$= \frac{V_s}{1 + \frac{R_s}{R_i}}$

If $R_i \gg R_s$

$V_i \simeq V_s$ - So i/p signal is not reduced

Voltage Amplifier Model

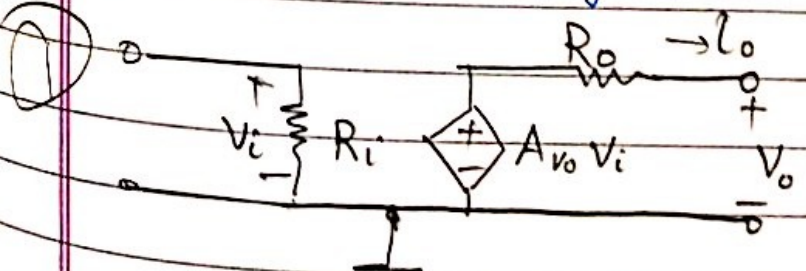
external



- Voltage V_i i/p } Voltage Voltage V_o o/p } Amplifier
- Current I_i i/p } Current Current I_o o/p } Amp.

i/p	o/p	
V_i	V_o	Voltage Amplifier
I_i	I_o	Current Amplifier
V_i	I_o	Transfer ratio = I_o/V_i = Trans conductance
I_i	V_o	" = V_o/I_i = Trans. Resistance

Voltage Amplifier's gain & ideal characteristics.



$A_{Vo} = \frac{V_o}{V_i} \Big|_{I_o = 0}$ &

$R_i \to \infty$, $R_o \to 0$.

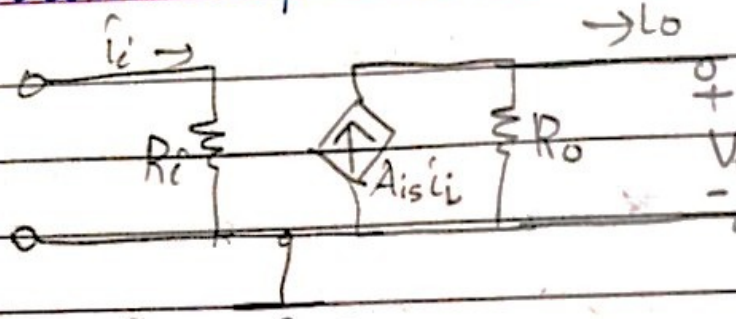
Voltage Amp.
OC Voltage Gain (A_{Vo})

Microelectronic Circuits Notes _ Akshansh

* Active device : can give out energy also
* Passive " : cant " " " .

• Current Amp Gain & Ideal char.

(2)



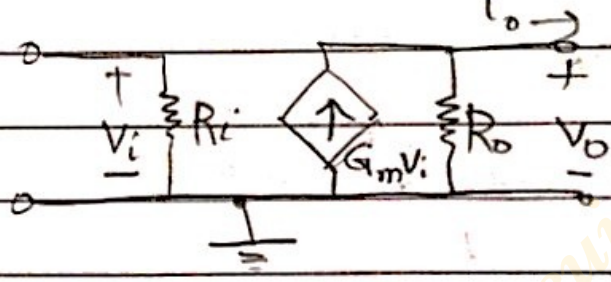
$$A_{io} = \frac{i_o}{i_s}\Big|_{V_o=0}$$

Current Amp.
SC Circuit gain (A_{is})

$R_i \to 0$ & $R_o \to \infty$

• Transconductance Amp. Gain & Ideal Char.

(3)

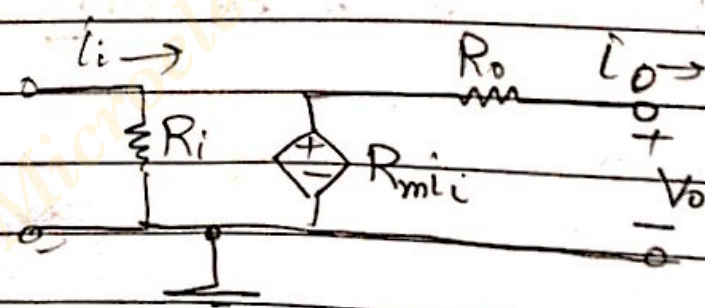


$$G_m = \frac{i_o}{V_i}\Big|_{V_o=0}$$ &

Transconductance Amp.
SC Transconductance (G_m)

$R_i \to \infty$ & $R_o \to \infty$

(4) • Transresistance Amp. Gain & Ideal Char.



$$R_m = \frac{V_o}{i_i}\Big|_{i_o=0}$$

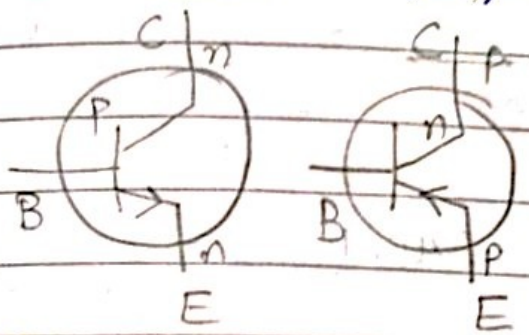
Transresistance Amp.
OC Transresistance (R_m)

& $R_i \to \infty$ & $R_o \to 0$

Microelectronic Circuits Notes - Akshansh

BJT

npn pnp



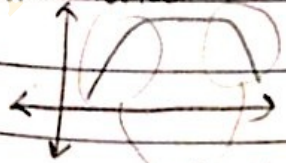
} Circuit Symbols.

Configuration	i/p	o/p
← CE (common emitter)	B & E	C & E
CB	E & B	C & B
CC	B & C	E & C

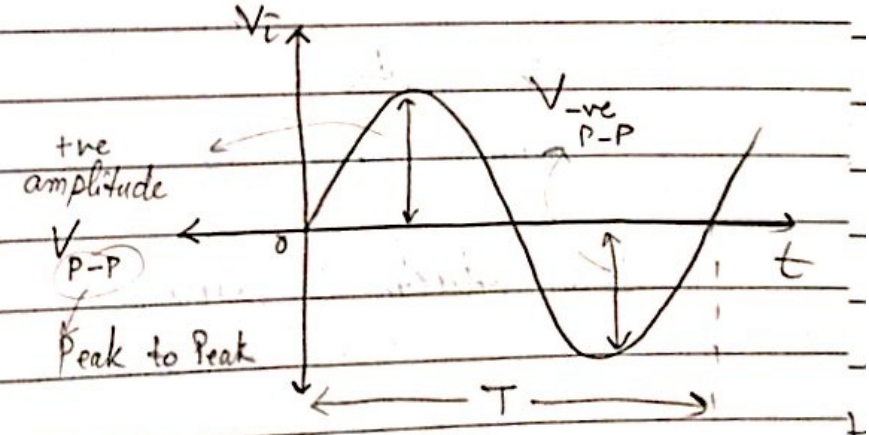
BJT as an amplifier

- fig 5.71
  - → See: i/p & o/p & the box (amplifier)
  - → graph

I am getting a gain like

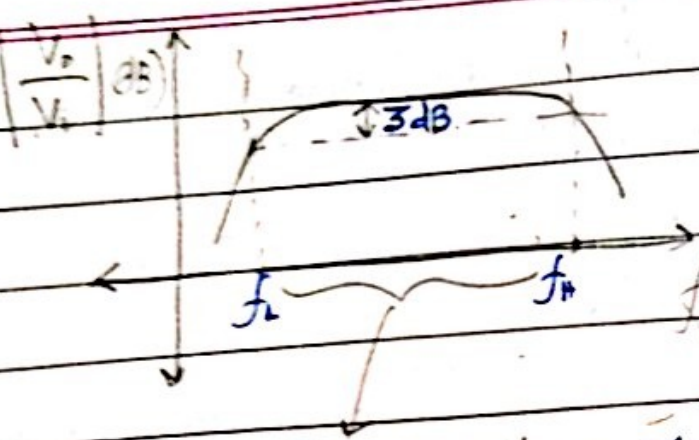


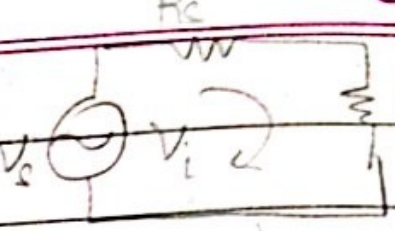
gain is falling. It's not uniform
Ideally we want it to be uniform throughout



Why is it not ideal?
∵ ∃ R_i & R_o : i/p & o/p resistances of amplifier.

Allaboutelectronic Circuits Notes - Akshansh





$$V_i = \frac{V_s}{\left(\frac{R_s}{R_i}\right)+1}$$

Stays constt = Mid Band = $f_H - f_L$

higher cut off frequency

lower cut off frequency

* Human ~~ear~~ ear will be able to sense an audio signal that is above 3 dB. So, on above graph, make a horizontal line, 3 dB down & the pt. of intersection gives f_H & f_L

- Problems to take care of :
  - Mid band gain (Voltage / Current / Power)
  - I/p & o/p resistances (R_{in} / R_{out})
  - Bandwidth = $f_H - f_L$
  - Small signal oper^n & large signal oper^n
- Self Study :- Amplifier : Some imp. defin^{ns} for use in analysis (see book)

Q. 1.39 Various amplifier & load combinⁿ are listed below using some values for each.

(a) Find voltage, current & power gains (A_v, A_i, A_p resp.) both as ratios & in dB.

(i) $V_I = 100mV$, $i_i = 100\mu A$, $V_o = 10\ V$, $R_L = 100\ \Omega$

(ii) $V_I = 10\mu V$, $i_i = 100mA$, $V_o = 2\ V$, $R_L = 10\ \Omega$

(iii) $V_I = 1\ V$, $i_i = 1mA$, $V_o = 10\ V$, $R_L = 100\ \Omega$

(i) $A_V = \frac{V_o}{V_i} = \frac{10}{100\times10^{-3}} = 100$ (no units)

in dB, its $20\log|A_v| = 20\log(100) = \underline{40\ dB}$

$A_i = \frac{I_o}{i_i} = \frac{V_o/R_L}{i_i} = \frac{10/100}{100\times10^{-6}} = 1000$.

in dB, $20\log(1000) = \underline{60\ dB}$

$A_p = \frac{V_o^2/R_L}{V_i/i_i} = \frac{V_o I_o / V_i I_i}{} = \frac{10\times(10/100)}{100\times10^{-3}\times100\times10^{-6}} = 10^5$

in dB, $10\log(10^5) = \underline{50\ dB}$

(ii) $A_V = \frac{V_o}{V_i} = \frac{2}{10\times10^{-6}} = 2\times10^5$.

in dB, $20\log(2\times10^5) = 20[\log 2 + \log 10^5]$

$= 20[0.3 + 5]$

$= 5.3 \times 20$

$= \underline{106\ dB}$

Microelectronic Circuits Notes_Akshansh

$$A_i = \frac{V_o/R_L}{i_i} = \frac{2/10}{100\times10^{-9}} = 2\times10^6$$

in dB $= 20\log(2\times10^6)$

$= 20[\log 2 + \log(10^6)]$

$= 20[0.3 + 6]$

$= 63\times2 = \underline{126\ dB}$

$$A_p = \frac{V_o I_o}{V_i i_i} = \frac{2(2/10)}{10\times10^{-6}\times100\times10^{-9}}$$

$$= \frac{4}{10^4}\times10^{15} = 4\times10^{11}$$

in dB $= 10\log[4\times10^{11}]$

$= 10[0.6+11] = \underline{116\ dB}$

(iii) $A_V = \frac{V_o}{V_i} = \frac{10}{1} = 10$, in dB $= 20$ dB

$$A_i = \frac{I_o}{i_i} = \frac{V_o/R_L}{i_i} = \frac{10/100}{10^{-3}} = 10^4$$

in dB $= 80$ dB

$A_p = A_V A_i = 10\times10^4 = 10^5$

in dB $= \underline{50\ dB}$

Ans

Microelectronic Circuits Notes - Akshansh

Q. Consider an amplifier ✓ operating from +/- 10 V power supply
✓ fed with sinusoidal voltage having 1 V peak
✓ delivers sinusoidal voltage o/p of 9 V peak to a 1 kΩ load
✓ draws a current of 9.5 mA from each of its 2 power supplies

Assume i/p current of amplifier is found to be sinusoidal with 0.1 mA peak. Find :-

(a) voltage gain
(b) current gain
(c) power gain
(d) power drawn from dc supplies
(e) power dissipated in the amplifier
(f) amplifier efficiency

(a) Voltage gain = $A_v = \frac{V_o}{V_i} = \frac{9}{1} = 9$

in dB = $20 \log(9) = 19.1$ dB

(b) Current gain = $A_i = \frac{i_o}{i_i} = \frac{9/1000}{0.1 \times 10^{-3}} = 90$

in dB = $20 \log(90)$

$= 20 [1 + 2(0.48)]$

$= 1.96 \times 20$

$= 39.2$ dB.

1.96
$\frac{0.2}{2.92}$

Microelectronic Circuits Notes - Anshansi

(c) Power gain, $A_p = A_v \cdot A_i$

$= 9(90) = 810$

in dB $= 10 \log(810)$

$= 10[1 + 4(0.48)]$

$= 29.2$ dB.

(d) $P_{dc} = V_{CC} I_{CC} + V_{EE} I_{EE}$

Power drawn from DC supply P_{dc} = 10 V, 9.5 mA

$= 2(10 \times 9.5 \times 10^{-3})$

$P_{dc} = 190$ mW.

(e) $P_{dissipated} = P_{dc} + P_i - P_L$

P_{dc} = 190 mW

$P_i = V_{i_{rms}} \cdot I_{i_{rms}} = \frac{V_i}{\sqrt{2}} \cdot \frac{I_i}{\sqrt{2}} = \frac{1 \times 0.1 \times 10^{-3}}{2}$

$= 0.05$ mW

$P_L = V_{o_{rms}} \cdot I_{o_{rms}} = \frac{V_o}{\sqrt{2}} \cdot \frac{I_o}{\sqrt{2}} = \frac{9 \times 9/1000}{2}$

$= 40.5$ mW

$\Rightarrow P_{dissi} = 190 + 0.05 - 40.5$

$= 149.55$ mW,

Microelectronic Circuits Notes - Akshansh

→ amplifier efficiency

(ii) $$\eta = \frac{P_L}{P_{dc}} \times 100$$

$$= \frac{40.5 \times 10^{-3}}{190 \times 10^{-3}} \times 100$$

$$= \frac{4050}{190} = 21.1\ \%$$

Ans

✱ BIASING OF BJT :-

≡ Addition of energy given to amplifier to help it amplify signal

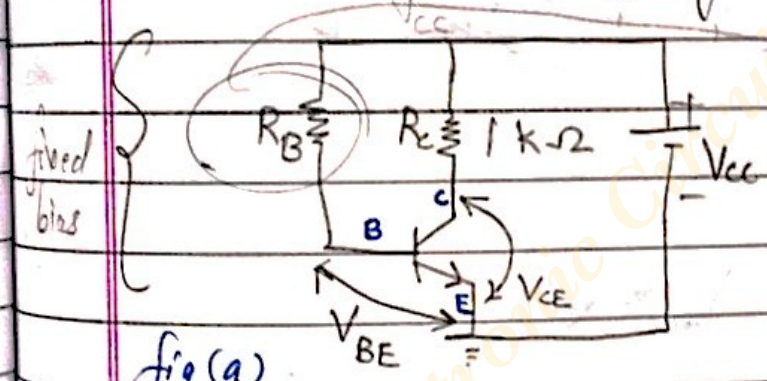


fig (a)

$$V_{B_2} = \frac{V_{cc} - V_{BE}}{R_B}$$

§ o/p characteristics of BJT

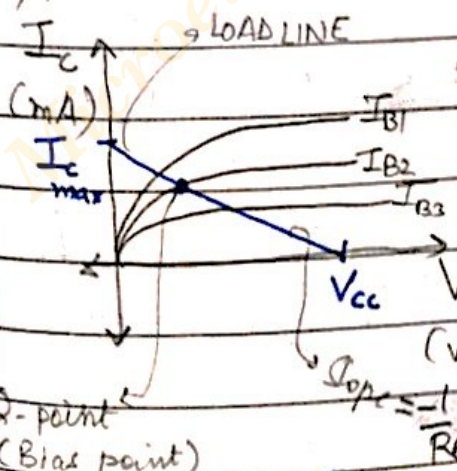


fig (c)

§ Self Biasing

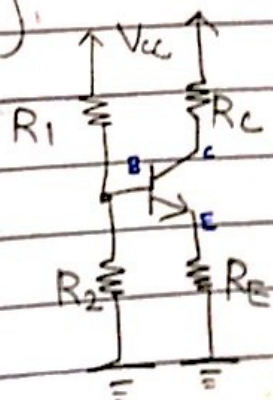


fig (b)

✱ Note: For any BJT (npn or pnp), E-B junction should be RB. & C-B junction should be FB

Microelectronic Circuits Notes - Akshansh

Puffin
Date
Page

* In the o/p charac. of BJT, we see that the Biasing pt. should be in the centre so that the signal can have a wide range to vary, in the linear region.
With temp change, the Q-pt. changes. We have to avoid that. So, use Stability factor.

- Lesser the value of stability factor (S), more stable the circuit is.
- Self bias : it automatically or just stabilises its bias pt. This method is preferable over fixed bias.

$V_B = \left(\frac{V_{cc}}{R_1+R_2}\right) R_2$ → fixed value.

eqns written from self biased circuit (prev pg)

$V_{cc} = I_c R_c + V_{CE} + (I_B + I_c) R_E$

$= I_c R_c + V_{CE} + I_c R_E$ (I_B negligible)

V_E

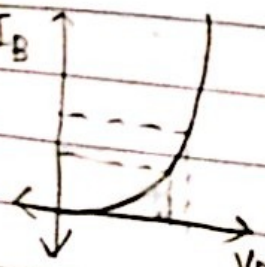
Fig (b)

Now, $V_{BE} = V_B - V_E$ → operating pt. has changed.

When T ↑, I_c ↑ ⇒ V_E ↑

Now, V_B is fixed.

So, V_{BE} will ↓ to keep V_B constt.



Now, seeing graph, small change in V_{BE} ⇒ large change in I_B

& $I_c = \beta I_B$

Now, as V_{BE} ↓ ⇒ I_B ↓

& ∵ I_B ↓ ⇒ I_c ↓

So, the increased I_c has been brought back to its pt. or the Q-pt. is

Microelectronic Circuits Notes - Akshansh

From previous pg. (under Biasing of BJT),

From fig (a), $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

(A) Graphical Analysis: find R_B Q-point.

From fig (c)

When $I_c = I_{c(max)} \rightarrow V_{CE} = 0$

$I_c = 0 \rightarrow V_{CE} = V_{CC}$

The pt. of intersection of these pts. is called as load line (Slope $= -1/R_C$)

Now, value of I_B will decide Q-point.

(B) Mathematical analysis: finding Q-point.

From fig. (b)

$V_B = \left(\frac{V_{CC}}{R_1+R_2}\right) R_2$: Voltage divider rule

: Neglecting value of I_B (very less)

Now, $I_E = I_B + I_C$

Now,

$V_E = (I_C + I_B) R_E$

Now,

$V_{BE} = V_B - V_E$

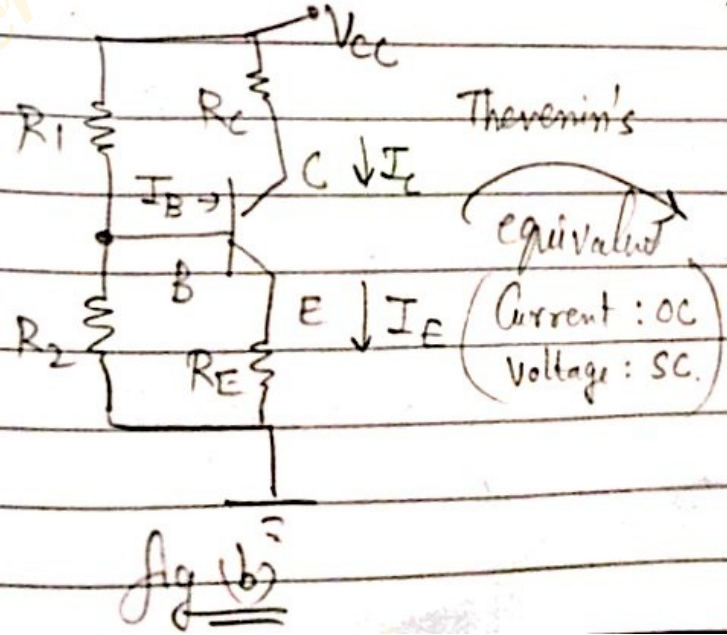


fig (b)

Thevenin's equivalent

(Current : OC
Voltage : SC.)

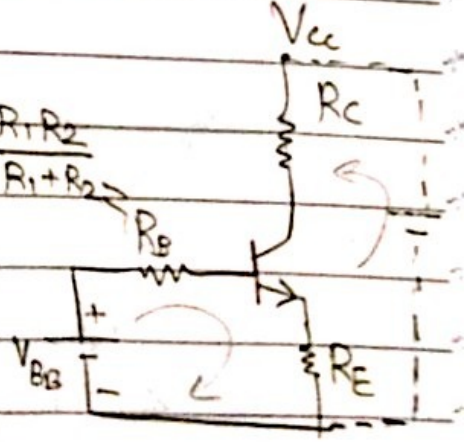


fig (d)

Microelectronic Circuits Notes - Avinash

Note:- for junction diodes:- $\alpha = \frac{I_C}{I_E}$; $\beta = \frac{I_C}{I_B}$

So, from fig (d), by KVL

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

$$\Rightarrow V_{BB} = I_B R_B + V_{BE} + (I_C + I_B) R_E \rightarrow (1)$$

KVL (in loop shown with dots)

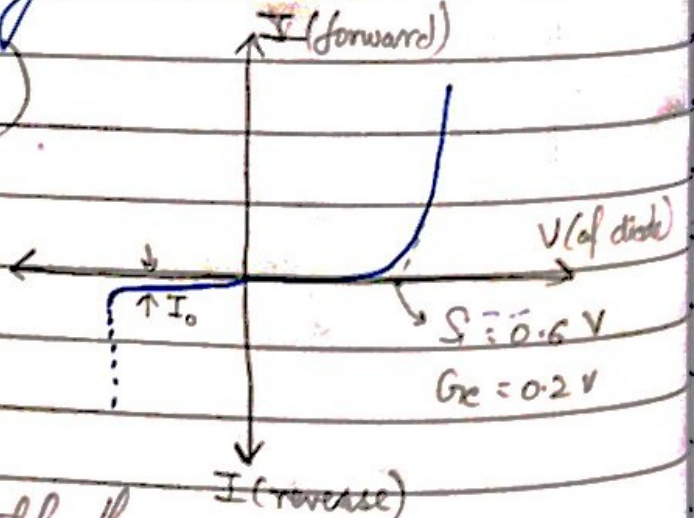
$$V_{CC} = I_C R_C + V_{CE} + (I_C + I_B) R_E \rightarrow (2)$$

with proper values given, eqn (1) & (2) can be evaluated to find values of V_{CE} & I_C. This will give a point on fig (c) - that pt. is Q-point

just for info. (done before)

* Characteristic of single junction diode:

$$I = I_0 \left(e^{V/\eta V_T} - 1 \right)$$



Now, making a BJT

metallurgically connecting both the diodes won't give us the BJT
∴ ∃ some gap between them & as carriers go from E to C, they'll die down in that gap.

* Resistance looked into the emitter : $r_e \equiv v_{be} / i_e$

$\Rightarrow \boxed{r_e = \frac{V_T}{I_E}}$

Lecture 5.6.1

Puffin
Date
Page

- Trans conductance & Collector Current

talking about o/p & i/p

$$v_{BE} = \underbrace{V_{BE}}_{DC} + \underbrace{v_{be}}_{AC}$$

$$i_C = I_S e^{v_{BE}/V_T}$$

$$= I_S e^{(V_{BE} - v_{be}/V_T)}$$

$$\Rightarrow i_c = (-I_c)\, e^{v_{be}/V_T}$$

Slope of transfer curve $\leftarrow$ $g_m = \left.\frac{\partial I_c}{\partial v_{BE}}\right|_{i_c = I_c}$

- Reading Assignment : Section 5.6.2, 5.6.3. See

Notations

	①	②	Component
(①) :	Small capital	capital capital	Complete (total)
(②)	Small	Small	DC AC. or instantaneous

* $V_T = \frac{T}{11600.} \simeq 26\,mV$ = Volt equivalent of temp. at RT

* $g_m = \left.\frac{\partial I_c}{\partial V_{BE}}\right|_{I_c = i_c}$ → Transconductance = slope of I_c vs V_{be} graph

* Resistance of BJT seen into the base (r_π) is defined as

$$r_\pi \equiv \frac{v_{be}}{i_b}$$

After solving, we get

$$\boxed{r_\pi = \frac{V_T}{I_B}} \quad (eqn\ 5.94)$$

Multielectronic circuit notes Akshansh

* Base : passive component
* Emitter : active component

$r_\pi = (1+\beta) r_e$	$g_m = \frac{I_C}{V_T}$	$r_\pi = \frac{\beta}{g_m}$

* ~~VCCS~~

BJT Small Signal Models :-

= Hybrid-π model.

Models: VCCS : Voltage Controlled Current Source ($g_m V_\pi$ version)
CCCS : Current Controlled Current Source (βI_b version)
} fig 5.51

= T-models.

VCCS & CCCS models.

($g_m V_\pi$ version, βI_b version)

Home Assignment (1) (deadline 26.2.13)

- Device fundamentals for BJT to work as amplifier
  - Students can refer to sub-section 5.3 : BJT as an amplifier.
- Obtain BJT's CE char. for Fairchild's BJT 2N3904 in PSPICE.
- Design BJT self-bias (scheme) circuit i.e, to obtain values of R_1, R_2 & R_E, the circuit shown in fig P5.130 (international version) → Same as in Assignment (2) written later

Given :- (a) Device is Fairchild's 2N3904
(b) Values of V_{cc} & R_c
(c) Manufacturer's datasheet of BJT (2N3904)

Microelectronic Circuits Notes - Vishnu

✓ Also, compute the model parameters of 2N3904 when used as the 4 models: a, b, c or d.

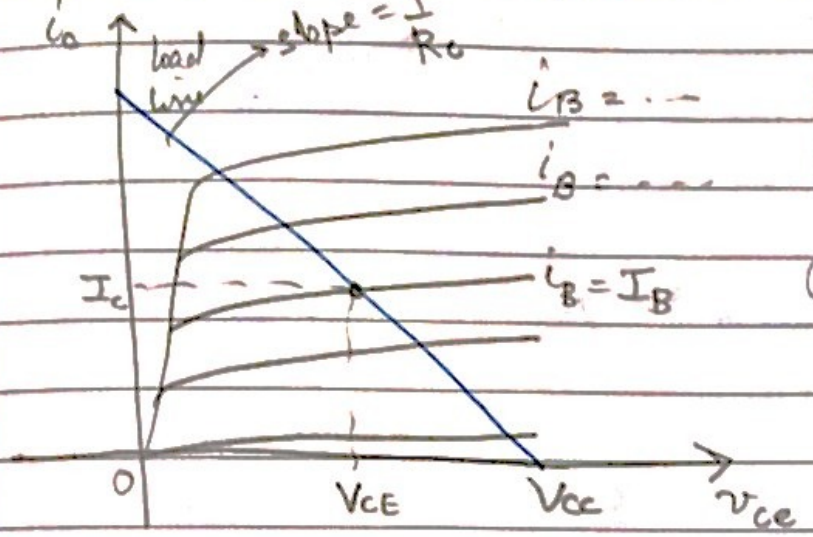


Fig 5.3.3 Graphical analysis for determining BJT's Bias Point (Q)

✱ BJT at high frequency model

= Hybrid-π model

- C_π : Emitter base junction capacitance
- C_μ : Collector base " "
- r_x : base spreading resistance

✱ Separating Signal & DC quantities.

- Every current & voltage in amplifier circuit is composed of :- ✓ dc component → for energising the device
  ✓ Signal component. → for transmitting acoustic signal.

∴ to separate DC & signal components : we need to amplify only signal component.

Microelectronic Circuits Notes - Akshansh

I_{CO} : reverse satur^n current when C-B junction is RB.

- Signal oper^n can be obtained by :-
  - ✓ eliminating DC sources (i.e, replace DC sources by SC)
  - ✓ replace DC current sources by OC.

- v_c : total instt. voltage at collector.

★ Voltage Gain, $A_V = \frac{-I_C R_C}{V_T}$ (see derivn)

Q Let $R_C = 2.2\ k\Omega$, $I_C = 2mA$, $V_T = 26mV$ at RT

$$A_V = \frac{-I_C R_C}{V_T} = \frac{2 \times 2.2 \times 10^{+3}}{26} \approx 170\ V/V$$

in Hybrid π & T models

★ EARLY EFFECT of BJT (effect not included)

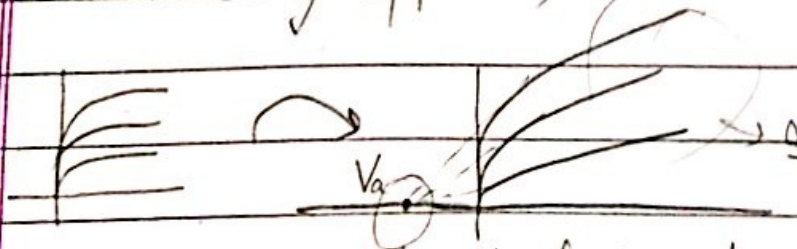
At a given value of v_{BE}, ↑ v_{CE} ↑ reverse bias voltage across J_C (junction b/w base & collector) & thus, ↑ increase width of depletion region. Thus, red^n in effective base width comes. (base width − depletion width)

As W (effective base width) decreases, I_S (reverse satur^n current) will ↑ & thus increasing i_C (proportionally)

Due to early effect,

$\because i_C = I_S e^{\cdots}$

As I_S ↑ ⇒ i_C ↑



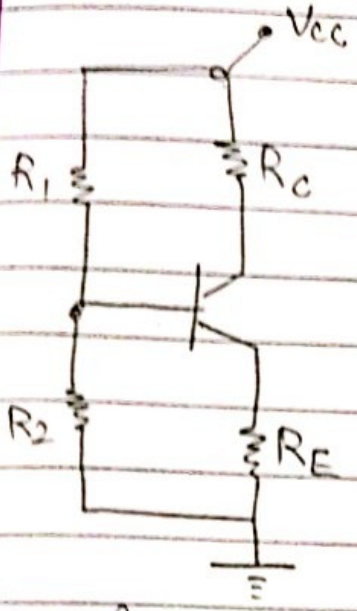
pt. of intersection, V_A = early voltage

So, to take its effect, put a resistance, r_o b/w C & E.

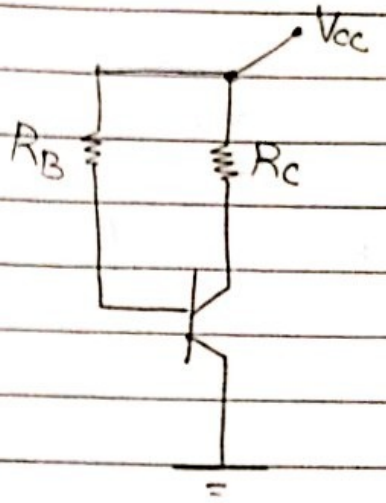
* BIASING a device in ACTIVE Region
⇓
EB junction: FB & CB junction: RB

Puffin
Date 21/2/13
Page

TUTORIAL no. 3



Self Bias Scheme



Fixed Bias Scheme

Q Evaluating Bias Stability for both schemes & proving that self bias scheme is superior to fixed bias scheme.

Stability factor, $S = \frac{\partial I_c}{\partial I_{co}}$ → a f^n of $I_{co}, \beta, v_{BE}, T \ldots$

→ β, v_{BE} : constt.
→ Basing on the basis of S value will also be true for S' & S''

Solving & we get,

→ R_1 parallel to R_2 } equivalent $= \frac{R_1 R_2}{R_1 + R_2}$

$S \simeq 1 + \frac{R_B}{R_E}$: for self bias scheme

& $S \simeq 1 + \beta$: for fixed bias scheme.
$\beta \to I_c/I_B$

→ exact expression :- $S = (1+\beta)\left(\frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}}\right)$ ★

Microelectronic Circuits Notes - Akshansh

Proof:- (for fixed bias)

$I_C + I_B + I_E = 0$ ——→ (1)

→ all currents into transistor is considered +ve

→ (supposed)

When BJT in active region,

$I_C = -(\alpha I_E - I_{CO})$ ——→ (2)

αI_E : reacting collector

I_{CO} : reverse satur"

Eliminating I_E from (1) & (2)

$\Rightarrow -(I_B + I_C) = \frac{-I_C + I_{CO}}{\alpha}$

$\Rightarrow I_C = -I_{CO} + \alpha(I_B + I_C)$

$\Rightarrow I_C(1-\alpha) = -I_{CO} - \alpha I_B$

$\Rightarrow I_C = \frac{I_{CO}}{1-\alpha} + \frac{\alpha I_B}{1-\alpha}$

Now, $\beta = \frac{\alpha}{1-\alpha}$

$\Rightarrow I_C = (1+\beta) I_{CO} + \beta I_B$ ——→ (4)

Now,

$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{\beta, V_{BE} \text{ const}}$

$\Rightarrow S = (1+\beta) + 0$

$\Rightarrow S = (1+\beta)$

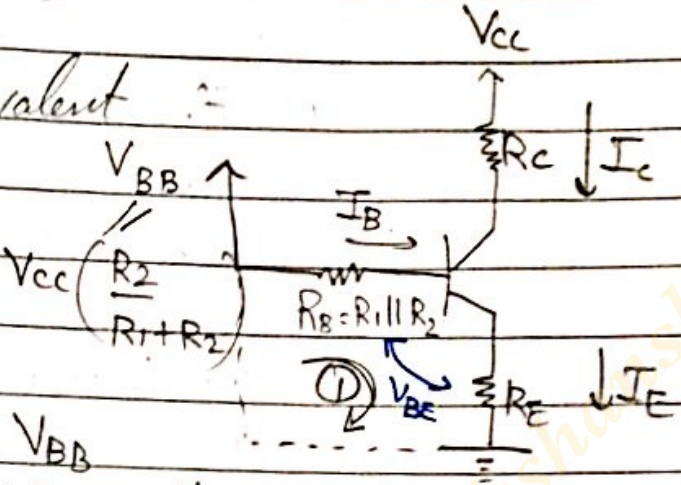
fixed bias

Microelectronic Circuit Notes - Akshansh

Puffin
Date
Page

Proof: (for self bias)

Taking Thevenin's equivalent :-



KVL on loop (1)

$$I_B R_B + V_{BE} + I_E R_E = V_{BB}$$

$$\Rightarrow I_B R_B + V_{BE} + (I_B + I_C) R_E = V_{BB} \longrightarrow (3)$$

Now, $I_C = (1+\beta) I_{CO} + \beta I_B \longrightarrow (4)$

Combining (3) & (4), we get

$$V_{BE} = V_{BB} + (R_B + R_E)\left(\frac{1+\beta}{\beta}\right) I_{CO} - \left(R_B + R_E(1+\beta)\right) I_C$$

Now, from (3), eliminating I_B,

$$I_B = \frac{V_{BB} - V_{BE} - I_C R_C}{R_B + R_E} \longrightarrow (5)$$

Using (5) in (4) & finding $S = \frac{\partial I_C}{\partial I_{CO}}$, we get

$$S = (1+\beta)\left(\frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}}\right)$$

After approxim^n, $S \simeq 1 + \frac{R_B}{R_E}$

Microelectronic Circuit Notes - Akshash

☆ Home Assignment (2) (deadline - 27.2.13)

- Design BJT self bias circuit (scheme) i.e., to obtain values of R_1, R_2 & R_E of the shaded part of the circuit shown in fig P5.130.

  Given :- (a) Device is Fairchild's 2N3904
  (b) Values of V_{cc} & R_c
  (c) Manufacturer's datasheet of BJT (2N3904)

- Note :- PSPice's Q.2N3904 is equivalent to Fairchild's 2N3904

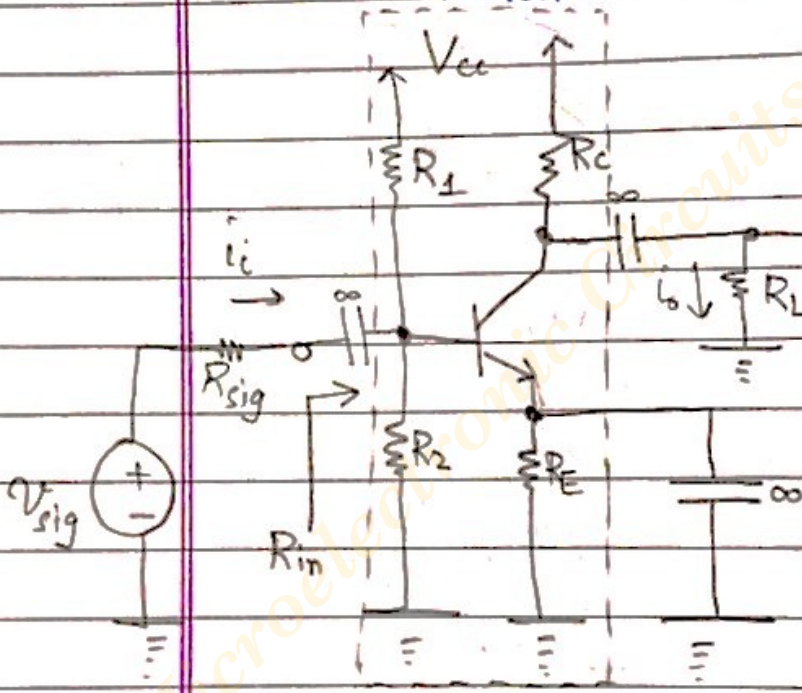


fig P5.130 BJT (CE) amplifier (with single power supply)

Same fig. as in assignment (1)

- controls Gain (V_o, I_o or A_v)
- R_c : collector resistance
- R_1, R_2, R_E : bias resistors
  → Try to FB EBJ RB CBJ
  → Hence, their selection decides posⁿ of Q-pt.

Microelectronic Circuits Notes Akshansh

Puffin
Date
Page

* In self bias, $S \simeq 1 + \frac{R_B}{R_E}$

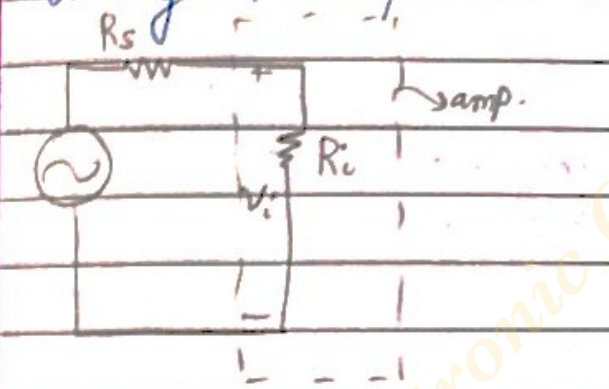
fixed bias, $S = 1 + \beta \frac{I_C}{I_B}$

So, we can change the resistance to bring min. stability factor.

But, $\beta \simeq 100$ or 1000. So, S becomes very large (for fixed bias circuit).

Hence, self bias preferable.

• Voltage transfer:

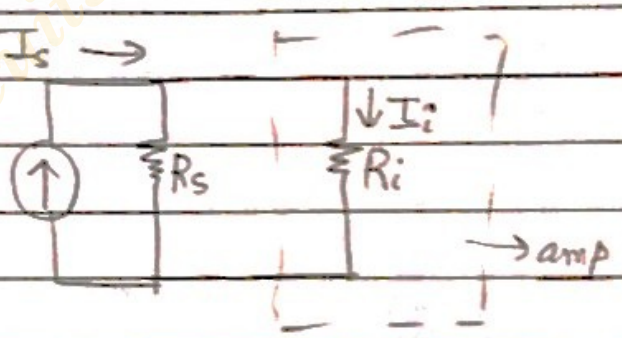


For source voltage, V_s to almost reach at V_i ($V_s \simeq V_i$), :

$R_i >> R_s$

(∵ R_s seems $\simeq 0$ & voltage becomes same)

• Current transfer



for $V_s \simeq V_i$,

$R_s \to \infty$ (∵ OC)

Practically not possible.

* So, $R_s >> R_i$.

Microelectronic Circuits Notes - Akshansh

- Common Emitter Amplifier
  - Assumptions
    - ✓ Capacitor ⇒ SC
    - ✓ All DC sources are shorted to ground.

Tutorial - 4

ASSIGNMENT - 3

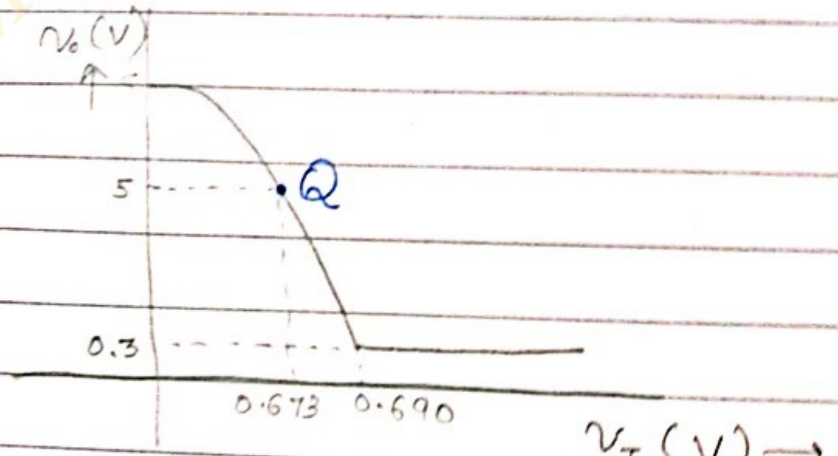
Ex 1.2 Pg-21 A transistor amplifier has transfer characteristics,

$$V_o = 10 - 10^{-11} e^{40 V_I}$$

which applies $V_I \geq 0\,V$

$V_o \geq 0.3\,V$.

(A) Find the limits L_- & L_+ & (B) the corresponding values of V_I. (C) Also find the value of the DC bias voltage V_I that results in $V_o = 5V$ & (D) voltage gain at the corresponding operating pt.



Microelectronic Circuits Notes - Akshansh

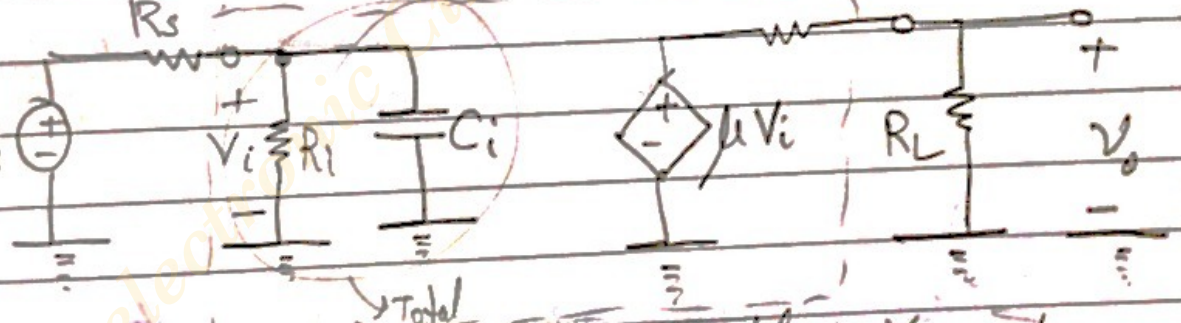
Ex-1.3 Fig 1.18

Pg 25

- Fig. is equivalent circuit of a 3-stage amplifier
- The amplifier is fed by a signal source resistance of 100 kΩ & delivers its o/p into a load resistance of 100 Ω
- Stage 1 has relatively high i/p resistance & a modest gain factor of 10
- Stage 2 has a higher gain factor but lower i/p resistance
- Finally stage 3, the o/p stage, has unity gain but low o/p resistance

Find overall voltage gain, V_L/V_s, current & power gain.

Ex-1.5



Total Resistance = Zi = Amplifier's i/p impedance

A voltage amplifier.

Find :- 1) Voltage gain, V_o/V_s as fn of frequency.
2) expression for DC gain & 3-dB frequency
3) for $R_s = 20\,k\Omega$, $R_i = 100\,k\Omega$, $C_i = 60\,pf$, $\mu = 144$, $R_o = 200\,\Omega$, $R_L = 1\,k\Omega$, Calculate :-
   (a) Dc gain
   (b) 3-dB frequency
   (c) frequency at which gain becomes 0 dB (i.e unity)

Microelectronic Circuits Notes_Akshaya

Sol^n (1) Applying voltage divider rule on

fig 1 $V_i = V_s \times \frac{Z_i}{Z_i + R_s}$ → (1)

fig 2 $V_o = (\mu V_i) \times \frac{R_L}{R_o + R_L}$ → (2)

Using (2) in (1)

$\Rightarrow V_i = \frac{V_o (R_o + R_L)}{\mu R_L}$

$\Rightarrow \frac{V_o (R_o + R_L)}{\mu R_L} = V_s \frac{Z_i}{Z_i + R_s}$

$\Rightarrow \frac{V_o}{V_s} = \frac{\mu R_L Z_i}{(R_o + R_L)(Z_i + R_s)}$

Answer req^d in some other form

Check # → $Z_i = R_i + \frac{1}{sC_i}$ → (3)

i.e. $Y_i = \frac{1}{R_i} + sC_i$ (Y_i → Admittance)

For a low pass STC network, the TF

$T(s) = \frac{K}{1 + s/\omega_0}$ → (A)

→ K : DC gain $= V_o/V_s$ at $s=0$

→ ω_0 : 3 dB frequency

→ $1/\omega_0 = \tau$: time constt.

Microelectronic Circuits Notes - Akshansh

From ①, using ③

$$V_i = \frac{V_s}{1 + R_s\left(\frac{1}{R_i} + sC_i\right)}$$

$$\Rightarrow V_i = V_s\left(\frac{1}{1 + \frac{R_s}{R_i} + sC_iR_s}\right)$$

$$= V_s\left(\frac{1}{1 + \frac{R_s}{R_i}}\right)\left(\frac{1}{1 + \frac{sC_iR_s}{1 + R_s/R_i}}\right)$$

$$V_i = V_s\left(\frac{R_i'}{R_s + R_i}\right)\left(\frac{1}{1 + \frac{sC_iR_iR_s}{R_s + R_i}}\right)$$

$$\Rightarrow \frac{V_i}{V_s} = \frac{R_i}{R_s + R_i}\left[\frac{1}{1 + \frac{sC_iR_iR_s}{R_s + R_i}}\right]$$

Now, from ②,

$$V_o = \mu V_i\left(\frac{R_L}{R_o + R_L}\right)$$

$$\Rightarrow V_i = \frac{V_o(R_o + R_L)}{\mu R_L}$$

$$\Rightarrow \left(\frac{V_o}{V_s}\right)\left(\frac{R_o + R_L}{\mu R_L}\right) = \frac{R_i}{R_s + R_i}\left[\frac{1}{1 + \frac{sC_iR_iR_s}{R_s + R_i}}\right]$$

$$\Rightarrow \frac{V_o}{V_s} = \left[\frac{\mu R_iR_L}{(R_s + R_i)(R_o + R_L)}\right]\left[\frac{1}{\left(1 + \frac{sC_iR_iR_s}{R_i + R_s}\right)}\right] \rightarrow (4)$$

Microelectronic Circuit Notes - Akshansh

- A_v = voltage gain = v_o / v_i
- G_v = voltage gain = v_o / v_{sig}

(2) Comparing (4) with (A), we get

$$K = \frac{\mu R_i R_L}{(R_o + R_L)(R_i + R_s)}$$

$$\omega_0 = \frac{R_i + R_s}{C_i R_i R_s} = \frac{1}{C_i (R_i \parallel R_s)}$$

Hence, we get $T(s) = \frac{K}{1 + s/\omega_0}$

$$\tau = \frac{1}{\omega_0} = C_i \cdot (R_i \parallel R_s)$$

(3) (a) DC gain, $K = \frac{\mu R_i R_L}{(R_o + R_L)(R_i + R_s)}$

$$= \frac{(144)(100 \times 10^3)(10^3)}{(200 + 1000)(100 \times 10^3 + 20 \times 10^3)}$$

$$= \frac{144 \times 10^8}{(1200)(120 \times 10^3)}$$

$$\Rightarrow K = 100 \text{ V/V}$$

(b) $\omega_0 = \frac{R_i + R_s}{C_i R_i R_s} = \frac{(100 \times 10^3) + (20 \times 10^3)}{(60 \times 10^{-12})(100 \times 10^3)(20 \times 10^3)}$

$$= \frac{120 \times 10^3}{12 \times 10^{-2}}$$

$$\Rightarrow \omega_0 = 10^6 \text{ rad/s}$$

(c) $\omega_0 = 2\pi f_0 \Rightarrow$ frequency, $f_0 = \frac{\omega_0}{2\pi} = \frac{10^6}{2\pi}$ Hz

Microelectronic Circuits Notes - Akshansh

↑ any amplifier

Puffin Date Page

✱ Steps in amplifier analysis :-

& analyse values of model parameters

S1) Determine DC operating pt. of BJT $\Rightarrow V_{CE}, I_C, I_B, I_E, V_{BE}$ .....

S2) Find values of g_m, r_π, r_e

S3) Replace DC voltage source → SC
DC current source → OC

S4) Replace BJT with ~~the current equivalent ckt~~ a model → hybrid-π or T-model.

S5) Redraw the circuit to get equivalent circuit.

eg $(-g_m V_\pi)(r_o \| R_C \| R_L) - g_o V_\pi (r_o - r_\pi = r_L)$

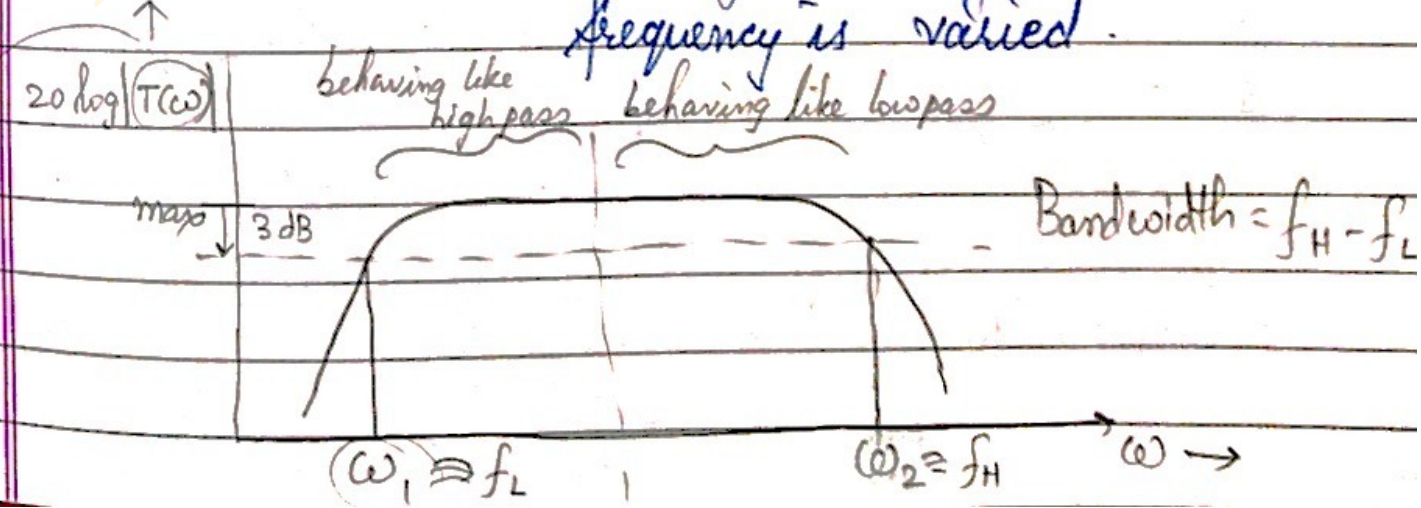
$= V_o$

$\Rightarrow \frac{V_o}{V_\pi} = (-g_m)(r_o \| R_C \| R_L) - g_o (r_o - r_\pi - r_L)$

Topic done ✱ Analysing different types of amplifiers (CE, CB, CC) to see their formulae & characteristics

✱ A_{is} : SC current gain ; ie A_i when o/p is SC

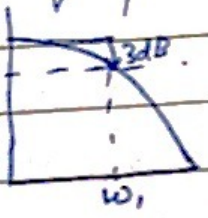
✱ Frequency response : the response got when the input voltage's (V_i signal) frequency is varied.



Microelectronic Circuits Notes - Akshansh

High pass : Passing from high V

* Lowpass ≡ frequency passing from low frequency area in graph

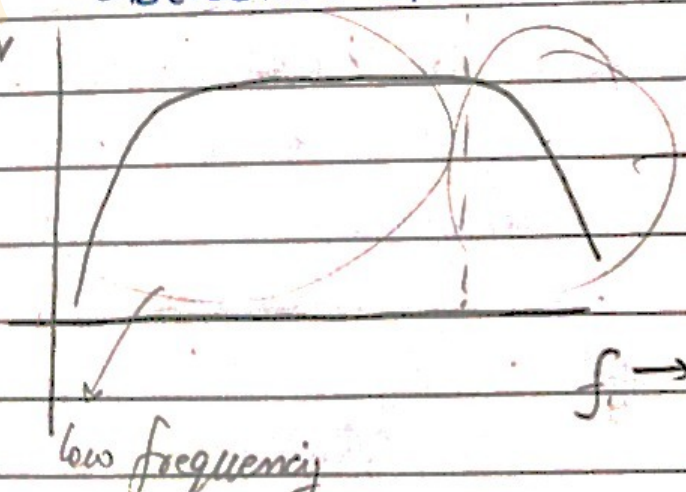


* STC circuit
Single time constant circuit : Tells how much signal falls from its full value to 1/e (≈66.6 %)
↳ T = RC

* R-C : Passive component : doesn't give gain
Amplifier : Active " gives gain
↳ when converted to RC network, its called : Active RC network

Q. Home assignment (4) , $f = \frac{1}{2\pi RC}$
Deriving TF for high pass & low pass

* DISCUSSION ON HIGH FREQUENCY MODEL



Microelectronic Circuit Notes Akshaya

~~High~~

At low frequency, $X_c = \frac{1}{2\pi f C}$

f is less. So, X_c is very high. So, it becomes an OC. So, C_μ & C_π (device capacitances) don't play any role in low frequency side. (only on high frequency side)

Hence,

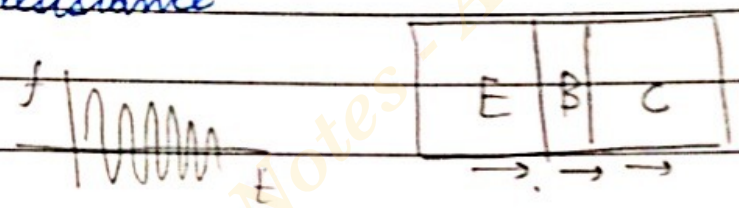
In high frequency model, r_x, C_μ & C_π come into picture.

C_π → Predominantly Diffusion capacitance

C_μ → Predominantly Transition capacitance

- r_x : base spreading resistance

⁂ Consider a wave



as $f \uparrow$, $\lambda \left(= \frac{c}{f}\right)$ decreases. So, the distance (λ) becomes comparable to the length of base

At low f, λ is very large

When f is high, the signal is non uniform. So, considering the section of base where signal is flowing, signal level at each pt. is diff^t. So, resistance is calculated in diff^t patches for each small pt. of base. Hence, for complete base, the avg. value is r_x.

At low frequency, signal is uniform, & λ has large value. So, r_x is a bulk resistance & hence, no need to take care for it.

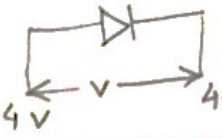
- form^n of capacitance due to diffusion (C_π) & trans^n (C_μ) in the base predominantly occur in high frequency model.

⁂ $C_\pi + C_\mu = \frac{g_m}{2\pi f_T}$ → I_C / N_T

f_T → unity gain cut off frequency (figure of merit)

After derivation

Microelectronic Circuits Notes - Akshansh

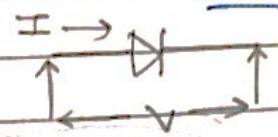
Note :- 

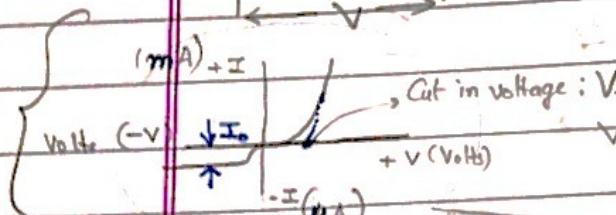
: Reverse Bias (∵ n side is at higher potential)

Puffin Date 5.3.13 Page

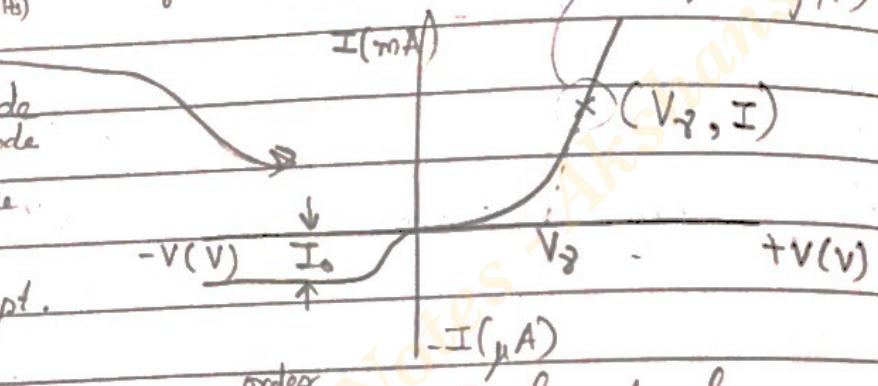
Concept : DIODE

The eqⁿ, $I = I_0 (e^{V/\eta V_T} - 1)$
↳ eqⁿ of diode
↳ I_0 : reverse saturⁿ current





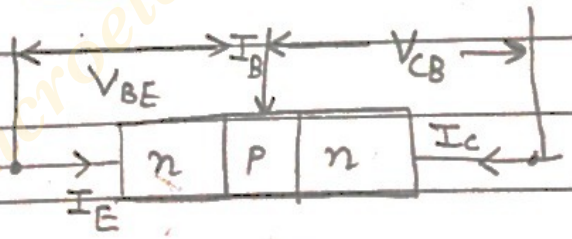
→ Characteristic curve of diode
→ I : current through diode
→ V : voltage across diode



R_F = Static resistance = $\frac{V}{I}$ at one pt. ; order ↝ few Ω's of ohms to few 100 Ω.

R_f = Dynamic resistance = $\frac{\Delta V}{\Delta I}$ at a Q-pt. ↝ ΔV is small & ΔI is very large, seeing graph.
↳ change in voltage across diode for current change
So, $R_f \overset{\text{order}}{\simeq}$ few ohms (very less than R_F)

BJT

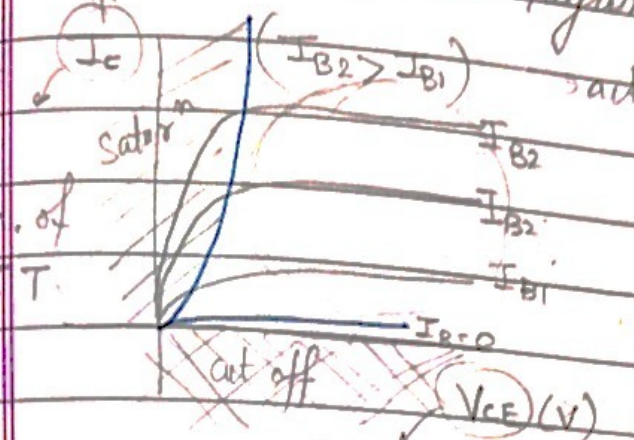


* Convention : Current going into transistor is taken as +ve dirⁿ
* Reverse saturⁿ current order :-
μ : Ge & n : Si
↳ micro ↳ nano

Nirjeetelectronics Circuits Notes - Akshay

Puffin
Date
Page

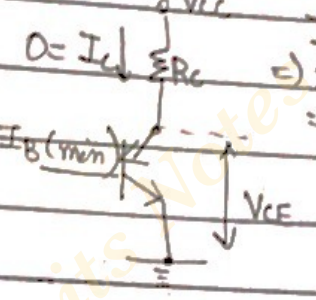
★ What are the voltages across junctions when a BJT is biased in its 3 regions (satur^n, active, cut off)



O/P Char. of BJT

≡ Seeing satur^n region :
It is near low value of V_{CE}
We find that in satur^n region, for every value of I_B, I_C is max & V_{CE} is min.

≡ Seeing cut off region :



$\Rightarrow I_C R_C = 0$
$\Rightarrow V_{CE} = V_{cc}$ for cut off region

≡ Seeing Active region :
I_C values vary from min to max
V_{BE} values should be greater & close V_γ
So, $V_{BE} \simeq 0.7$ V (Si)

Junctions :	J_E	I_C
Active Region	FB	RB
Cut off	RB	RB
Satur^n	FB	FB

★ Help us know the region in which BJT acts.

Example 5.2

Q. In a CE circuit, $I_S = 10^{-15}$ A. A collector resistance $R_C = 6.8$ kΩ & a power supply $V_{cc} = 10$ V.

(a) Determine V_{BE} to operate the BJT at $V_{CE} = 3.5$ V & also find I_C (collector current)

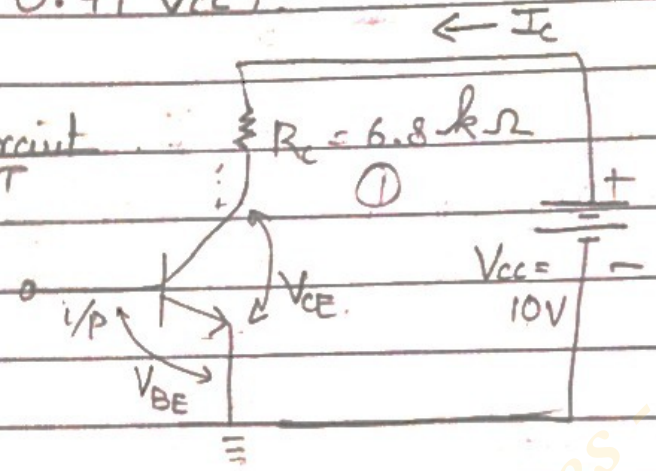
(b) Find A_v at this bias pt.
If 5 mV (V_{peak}) sine wave (sinusoidal wave) is superimposed on V_{BE}, determine amplitude of o/p sine wave.
(Assume linear oper^n)

Microelectronic Circuits Notes Arcansis

* In this case, at i/p, only V_T is available.

(c) To drive the BJT to the edge of saturation, where $v_{CE} = 0.3\,V$, determine needed increment in v_{BE}.

(d) To drive the transistor to within 1% of cut off ($v_O = 0.99\,V_{CC}$)



(a) (KVL) $+V_{CC} - V_{CE} - I_C R_C = 0$

① $10 - 3.5 - I_C(6.8 \times 10^3)$

Finding I_C

$\Rightarrow \dfrac{6.5}{6.8 \times 10^3} = I_C$

$\Rightarrow I_C = 0.9558\ mA$

Finding V_{BE}

$I_C = I_S e^{V_{BE}/V_T} = 10^{-15} e^{V_{BE}/26\,mV} = 10^{-3}$ (or, take 25 mV)

$\Rightarrow 10^{12} = e^{V_{BE}/26\times10^{-3}}$

$\Rightarrow 27.63 = \dfrac{V_{BE}}{26\times10^{-3}} \Rightarrow V_{BE} = 0.718\,V$

(b) $A_v = -\dfrac{V_{CC} - V_{CE}}{V_T} = -\dfrac{(10-3.5)}{26\times10^{-3}} = -250\,V/V$

or $-\dfrac{I_C}{V_T}(R_C)$

Amplitude of o/p sine wave $= A_v\, 5\,mV$

$= -1.25\,V.$

Microelectronic Circuits Notes - Akshansh

(c) $v_{CE} = 0.3\ V$.

Now, $i_C = \frac{V_{CC} - v_{CE}}{R_C}$ (KVL)

$\Rightarrow i_C = \frac{10 - 0.3}{6.8 \times 10^3}$

$\Rightarrow i_C = 1.426\ mA$

$\Delta v_{BE} = V_T \ln\left(\frac{i_C}{I}\right)$ $\left(\because i_C = i_0\left(e^{\Delta V_{BE}/V_T} - 1\right)\right)$

ΔV_{BE} ✓

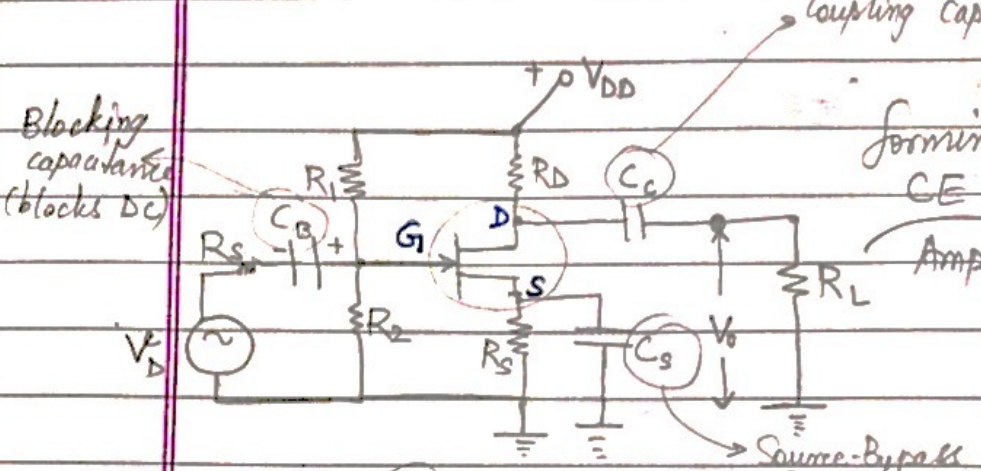
#

HW

Microelectronic Circuits Notes_Akshansh

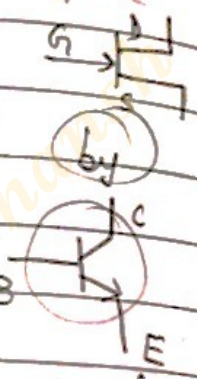
Date 10.3.13
Page

8h - MOSFET



forming CE Amplifier

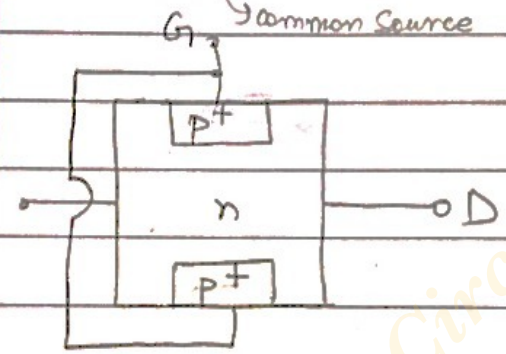
Replace by

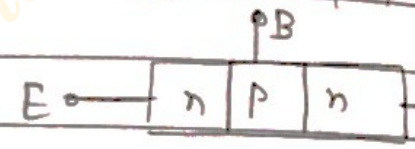


JFET (CS) Amplification

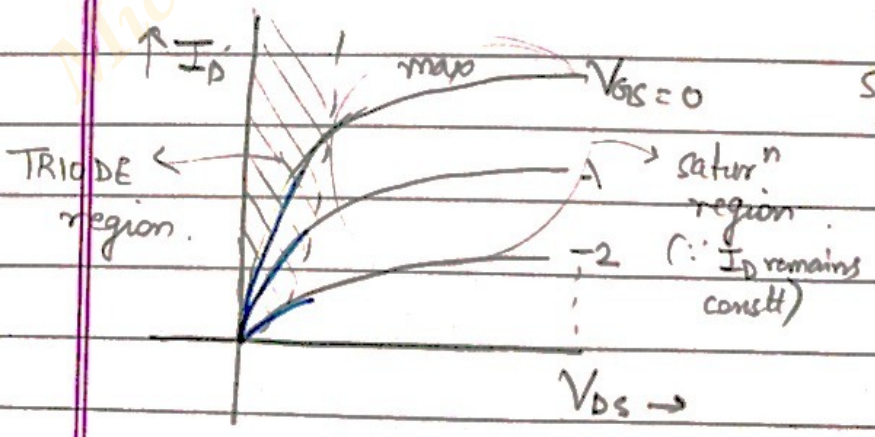
(CE Amplifier)

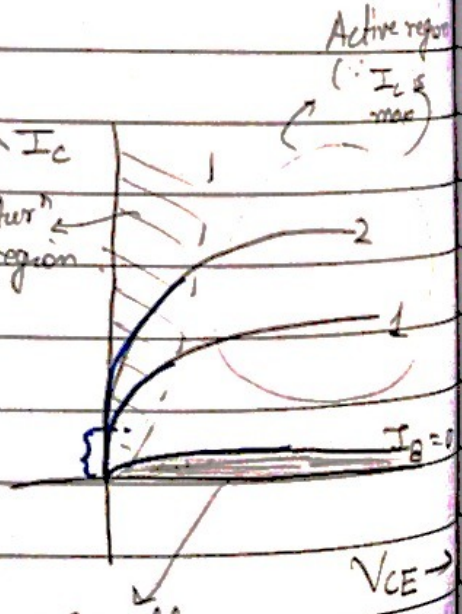
common Source





- ✓ has only 1 junction.
- ✓ When RB is applied across G & S, channel width reduces (due to depletion region form^n). So,
- ✓ characteristic curve





Microelectronic Circuits Notes - Akshay

★ FET is known for its noise immunity.
(∵ in BJT, o/p ∃ even when i/p is zero.
Seeing fig, when $V_{CE} = 0$, still, ∃ some value of I_C. So, ∃ noise)
In case of FET, the graph shows that all lines pass through origin. So, at origin, ∃ no value. So, o/p ∄ when i/p = 0.

- Moreover, there is difference in resistance in BJT & FET.

Microelectronic Circuits Notes - Akshansh

Example 4.11

Q A transistor amplifier is fed with a signal source having OC voltage, $v_{sig} = 10\,mV$ & internal resistance, $R_{sig} = 100\,k\Omega$, the voltage i/p & o/p of amplifier are measured with & without R_L (both of them), where $R_L = 10\,k\Omega$.

v_i (mV)	v_o (mV)	
9	90	without $R_L \Rightarrow R_L \to \infty$
8	70	with R_L

Find: All the amplifier parameters:

(a) R_i, R_{in}, R_{out}, R_o

(b) A_v, A_{vo}

(c) A_i

(d) G_m, G_{vo}, G_v

(b)

$$A_{vo} = \frac{v_o}{v_i} \text{ (without } R_L) = \frac{90}{10} = 9$$

$$A_v = \frac{v_o}{v_i} \text{ (with } R_L) = \frac{70}{8} = 8.75$$

(d) $$G_{vo} = \frac{v_o}{v_{sig}} \text{ (without } R_L) = \frac{90}{10} = 9 \text{ V/V}$$

$$G_v = \frac{v_o}{v_{sig}} \text{ (with } R_L) = \frac{70}{10} = 7 \text{ V/V}$$

(a) We know

$$G_{vo} = \frac{v_o}{v_{sig}} \times A_{vo}$$

$$\Rightarrow G_{vo} = \left(\frac{R_i}{R_i + R_{sig}}\right) \times A_{vo}$$

$$\Rightarrow 9 = \left(\frac{R_i}{R_i + 100}\right) \times 10 \Rightarrow R_i = 100\,k\Omega$$

Microelectronic Circuits Notes Akshansh

$$A_v = A_{10} \frac{R_L}{R_L + R_o}$$

$$\Rightarrow 8.75 = 10 \left[\frac{10}{10 + R_o} \right]$$

$$\Rightarrow R_o = 1.43\ k\Omega.$$

HW 2

Microelectronic Circuits Notes - Akshansh

IC BIASING

↳ ⇒ applying a constt current source
↳ a constt DC current (I_{REF}) generated at one loc^n of IC chip, utilizing a precision resistor external to IC chip.

- Current steering: a process by which I_{REF} is replicated for biasing several stages.

how it is done

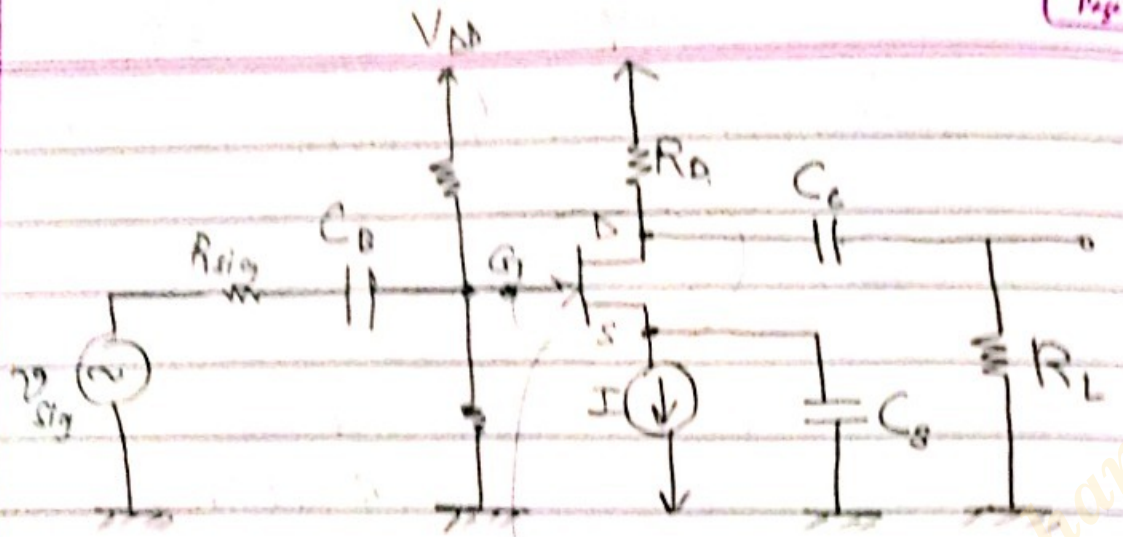
* Basically, we are aiming at using an I.C (internal circuitry), instead of external wires (done before) for Biasing.

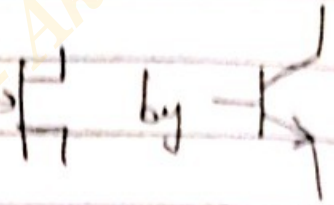
So, an external part (Voltage + Resistance ↝ gives current, I_{REF}) giving current is used in many areas of IC

- This is done for FET's

* Precision Resistor:
has a tolerance of ±1% by changing any property of resistor (eg. temp, current through it)

* Ulg, other defin^{ns} :- Precision Diode, Precision ...



> replace →  by

(CE Amp.)

Idea :- Current generated at one place is duplicated throughout the device.

✱ ACTIVE LOAD

- Presence of active device at load.
  - → eg : BJT, FET
- Initially, passive load (resistance $R_D \| R_L$) are connected. For large resistance req'd, we'll need to have more length. So, using this in IC, the size of circuit increases → not advisable. So, it cannot be realised.
  So, MOSFET as a VVR (Voltage variable Resistance) can be used in its place (∵ MOSFET behaves as VVR in TRIODE region).

Microelectronic Circuits Notes - Akshansh

Example 6.14

Q. Find A_0 (Transfer gain), fabricated in a 0.4 μm CMOS process, for which $k_n' = 200\ \mu A/V^2$ & V_A' (early voltage) = 20 V/μm.

The transistor has a channel length = 0.4 μm & is operated with an over drive voltage, $V_{ov}\ (= V_{GS} - V_{tn})$ of 0.25 V.

What must be w for the n-MOS transistor to operate at $I_D = 100\ \mu A$

Also find value of g_m & r_o

→ or Intrinsic gain $(= g_m r_o)$

We know:- $\boxed{I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2}$ → V_{ov}

$$\Rightarrow 100\ \mu A = \frac{1}{2}(200\ \mu A)\left(\frac{W}{0.4\ \mu m}\right)(0.25)^2$$

$$\Rightarrow 200\ \mu A = (200\ \mu A)\left(\frac{W}{0.4\ \mu m}\right)(0.25)^2$$

$$\Rightarrow 0.4 \times 10^{-6} = W (0.25)^2$$

$$\Rightarrow W = 6.4\ \mu m$$

Now,

$g_m = 0.8\ mA/V$. (using its formula)

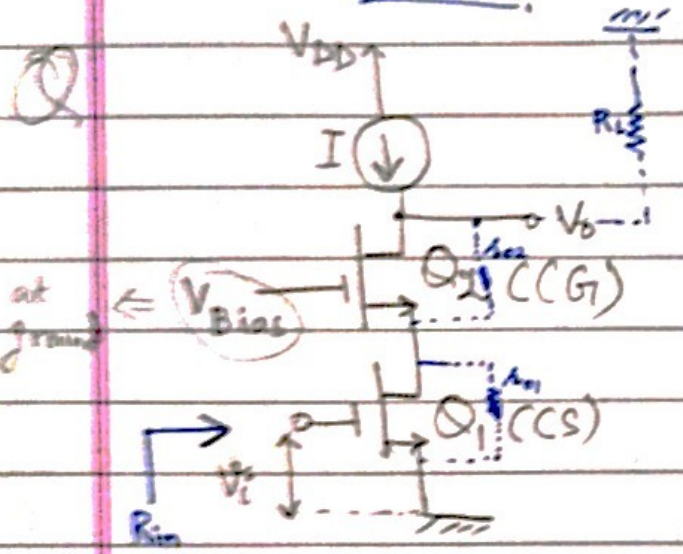
HW

Microelectronic Circuits Notes - Akshansh

CMOS Implementation of common source amplifier

$$A_v = \frac{v_o}{v_i} = A_{vo} \cdot \frac{R_L}{R_L + R_o}$$

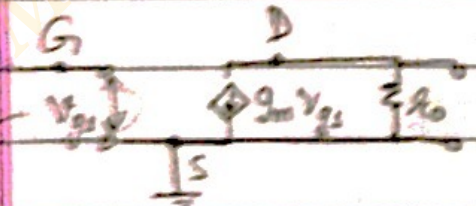
MOS CASCODE



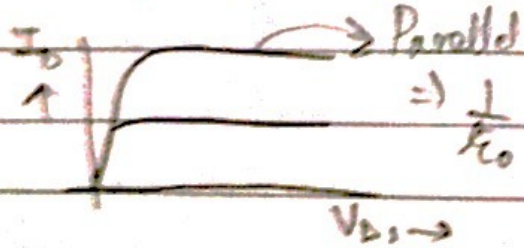
Transistor Q1 is connected in common source config & provides its o/p to i/p terminal of transistor Q2. Transistor Q2 has a constt DC voltage, V_{bias}, applied to its gate, thus, the signal voltage at the gate of $Q_2 = 0$ & Q_2 is operating as common gate amp with a constt current load I. In both Q_1 & Q_2, the drain current = I. The common gate transistor, Q_2 is called CASCODE transistor & the fig. shows MOS CASCODE Amplifier.

Find :-
Analyse this to get voltage gain, R_{in} & R_{out}

Using hybrid-π model for Q1



In case of I_D vs V_{DS} characteristic



$\Rightarrow \frac{1}{r_o} = 0 \Rightarrow r_o \to \infty$.
$\Rightarrow R_{in} \to \infty$.

} Ideal MOS Amp.

In response to i/p signal voltage v_i, CS transistor Q1 conducts a current signal ($g_{m1} v_i$) in its drain terminal & feeds it to the source terminal of CG transistor, Q2.

The transistor Q2, passes signal current ($g_{m1} v_i$) onto its drain, where, it is supplied to a load R_L.

Now,

$$R_{out} = \underbrace{r_{o2}}_{\text{i/p resistance for } Q_2} + A_{vo} \underbrace{r_{o1}}_{\text{o/p resistance for } Q_1}$$

$$\simeq (g_{m2} r_{o2}) r_{o1}$$

At the drain of Q1, looking downward, we see o/p resistance of CS Amp, Q1, which is r_{o1}.

Looking upward, we see i/p resistance of CG transistor, Q2.

$$\text{So, } R_{in2} = \frac{1}{g_{m2} + g_{mb2}} + \frac{R_L}{A_{vo2}}$$

$$\hookrightarrow A_{vo2} = 1 + (g_{m2} + g_{mb2}) r_{o2}$$

Thus, the total resistance b/w drain of Q_1 & ground is $R_{d1} = r_{o1} \,//\, \left[\left[\frac{1}{g_{m2} + g_{mb2}}\right] + \frac{R_L}{A_{vo2}}\right]$

$$\text{So, } R_{out} = r_{o2} + A_{vo2} \cdot r_{o1}$$

which has been obtained, noting source resistance R_s is o/p resistance, r_{o1} of Q1.

Substituting for A_{vo2} $\left[= 1 + (g_{m2} + g_{mb2}) r_{o2}\right]$

we get $R_{out} = r_{o2} + \left(1 + (g_{m2} + g_{mb2}) r_{o2}\right) r_{o1}$

Microelectronic Circuits Notes - Akshansh

Noise ≡ * EMI : Electro Magnetic Interference Signal

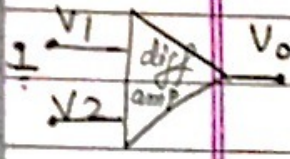
Puffin Date 26/3/22 Page

which can be approximated as

$R_{out} \simeq g_{m2} r_{o2} r_{o1}$

CHAPTER-7

DIFFERENTIAL AMPLIFIER



→ an amplifier that tries to amplify the diff. b/w i/p & o/p signals

→ consider a sys where the difference is very small. In order to analyse it (using devices like galvanometer, ⇒) we need these differential amplifiers.

→ every source has some common signals. If we take diff. the common signals become zero & noise is prevented

→ used in ECG

→ V_d : difference voltage ; V_c : common mode vol. → avg. of 2 signals

→ A_d : differential / difference gain

By defin^n :-

$$V_d = V_1 - V_2 \quad \& \quad V_c = \frac{1}{2}(V_1 + V_2) \Rightarrow \begin{cases} V_c + \frac{V_d}{2} = V_1 \\ V_c - \frac{1}{2}V_d = V_2 \end{cases}$$

Now, $V_o = A_d (V_1 - V_2)$

Now, $V_o = A_1 V_1 + A_2 V_2$ (POS)

Considering the o/p signal as :- Sum of differential mode signal & common mode signal (POS)

$$\Rightarrow V_o = A_d V_d + A_c V_c \longrightarrow (2)$$

Microelectronic Circuits Notes - Akshansh

Puffin
Date
Page

// ly, $A_d = \frac{1}{2}(A_1 - A_2)$ & $A_c = A_1 + A_2$

→ Common Mode Rejection Ratio (CMRR)

$$\therefore \boxed{\rho \triangleq \frac{A_d}{A_c}} \quad (\text{in dB})$$

$$\Rightarrow v_o = A_d v_d + \frac{A_d}{\rho} \cdot v_c \quad (\text{from } ②)$$

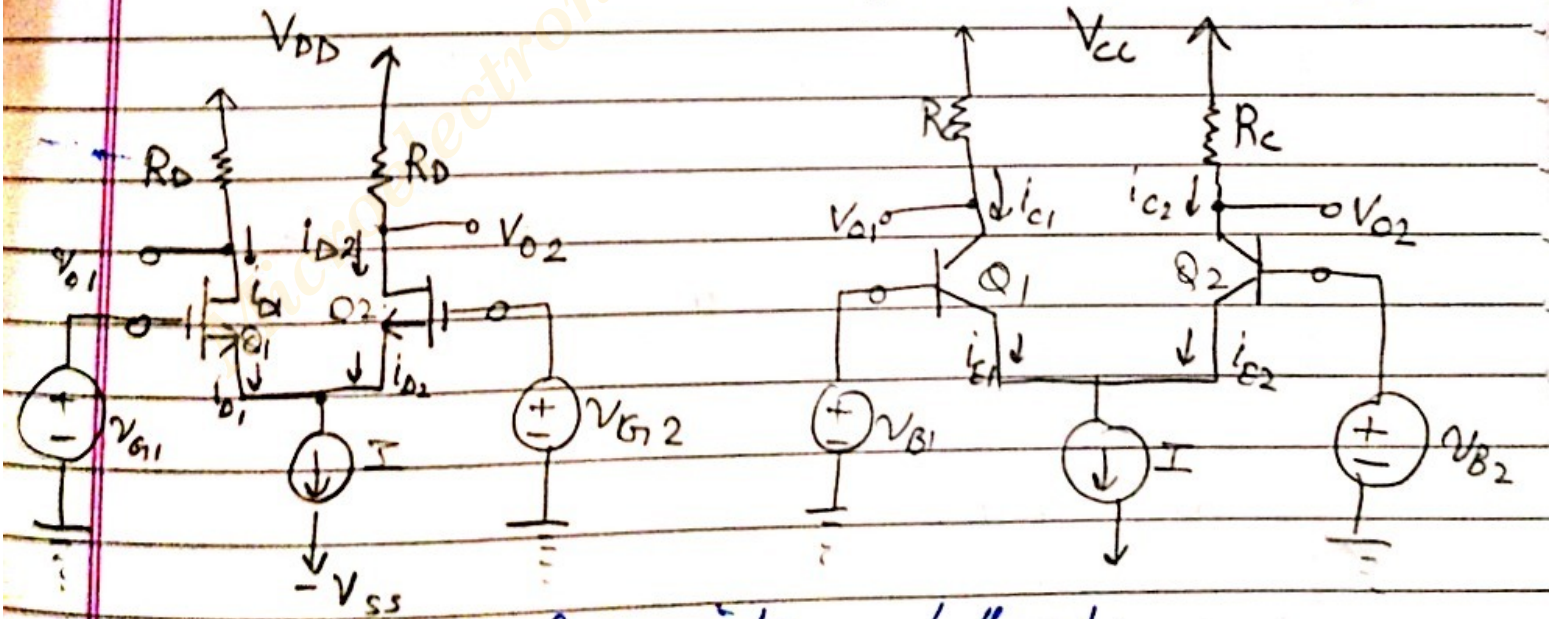
$$\Rightarrow V_o = A_1 V_d \left[1 + \frac{V_c}{\rho V_d} \right]$$

→ I want $v_o = A_d v_d$: ideally.

$\Rightarrow \rho \to \infty$

$\Rightarrow$ CMRR should be very large.

☆ Basic MOS & BJT differential pair config.



→ of the transistors on both sides

- All (device parameters must be the same (exactly) : called as Matching Transistors.

Electronic Circuits Notes | Akshansh

Fig. 7.2 (Same as prev. pg. fig. of MOSFET)
with $i_{D_1} = i_{D_2} = I/2$

$V_s = V_{CM} - V_{GS}$ → the voltage corresponding to $I/2$

Neglecting channel length modul",

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

Or, in terms of overdrive voltage,

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{OV})^2$$

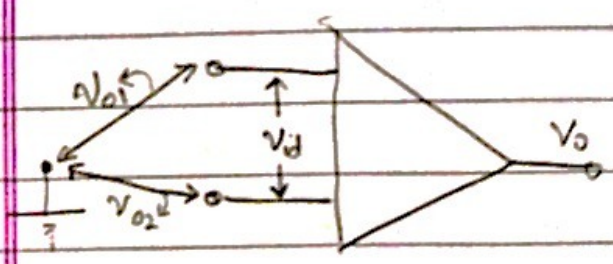
$$\Rightarrow V_{OV} = \sqrt{\frac{1}{k_n' (\frac{W}{L})}}$$

Where, voltage at each drain is :-

$$V_{D1} = V_{D2} = V_{DD} - \frac{1}{2} R_D.$$

$\therefore (V_{D1} \sim V_{D2}) = 0$!

↳ Differential pair rejects c.m signal.



none of i/p terminals are at GND

✓ $V_c = \frac{V_{o1} + V_{o2}}{2}$

✓ $A_c = \frac{V_o}{V_c}$

✓ $A_d = \frac{V_o}{V_d}$

Microelectronic Circuits Notes - Akhansh

→ In earthquakes, ∇ is low. So, low ∇ models are used.

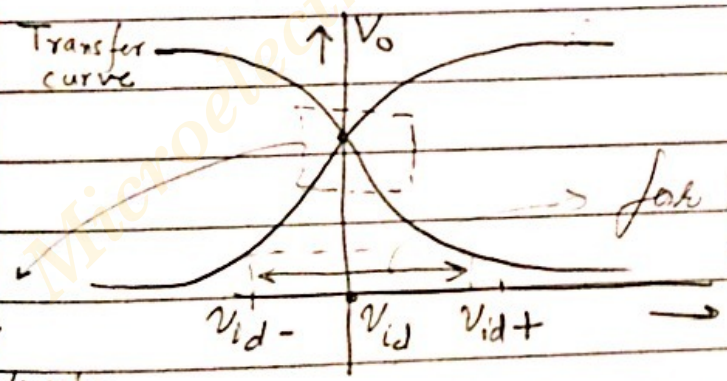
Puffin
Date
Page

Applic^n

☆ OP-AMP has 4 stages of its working
↳ 1st 2 stages: Differential amp.
(2 differential amps in cascade
1st stage :- Differential ended : i/p
" " : o/p
2nd stage :- Differential ended : i/p
Single ended O/P

* Procedure of differential amp :-
Same for normal amp.

☆ ASSIGNMENT : (6)
Analyse the differential amplifier and find expressions & device parameters (including CMRR...).
Also find: transfer characteristics.
↳ o/p parameter
i/p parameter



→ for 10 of volt
(max value is V_{cc})

linear characteristic
(linearity can be extended)

Microelectronic Circuits Notes Akshansh

TEST 1

PART-B

Q.1 BJT high Π model : directly from textbook

$C_\Pi = C_{de} + C_{je}$

$C_{de} = \tau_F g_m$

$\Rightarrow C_{de} = \tau_F \frac{I_c}{V_T}$

$C_{je} = 2 C_{je0}$

$C_\mu = \frac{C_{\mu 0}}{\left[1 + \frac{V_{CB}}{V_{OC}}\right]^m}$

Ans :-

$C_\Pi = 0.53\ pF$

$C_\mu = 12.7\ fF$

Q.2 From given fig

$I_D = 1mA$, $V_D = 3V$ } given, & $R_D = \frac{V_D}{I_D} = 3k\Omega$

$V_S = V_{SS} - I_D R_S$ (KVL)

($V_{SS} = 10V$ Given)

By voltage divider rule, $V_G = \frac{R_2}{R_1 + R_2} \cdot V_{SS}$

Given, 10A current in voltage divider,

$\Rightarrow \frac{V_{SS}}{I} = R_1 + R_2 \Rightarrow R_1 + R_2 = 1\Omega$

($V_{SS} = 10V$, $I = 10A$)

Microelectronic Circuits Notes - Akshansh

* for pMOS, V_t is -ve

Puffin
Date
Page

Now, $I_D = \frac{1}{2} k_p' \left(\frac{W}{L}\right) (V_{GS} + V_t)^2$

I_D → 1 mA (Given)

k_p' → 0.6 mA/V²

$\left(\frac{W}{L}\right)$ → ?

$|V_t| = 1$

$\Rightarrow V_t = -1\ V$ ($\because$ it's pMOS)

$\Rightarrow V_{GS} + 1 = 1.82$

$\Rightarrow V_{GS} = -2.82\ V$.

Given, $V_D = 3V$

$V_{DS} = V_{GS} - V_t - 1$

$= -2.82 + 1 - 1 = -2.82\ V$.

$V_{DS} = V_D - V_S$

$\Rightarrow V_S = V_D - V_{DS} = 3 - (-2.82) = 5.82\ V$

$\Rightarrow R_s = \frac{V_{SS} - V_S}{I_D} = \frac{10 - 5.82}{I_D} = 4.18\ k\Omega$

& $V_{GS} = V_G - V_S$

$\Rightarrow -2.82 = V_G - 5.82$

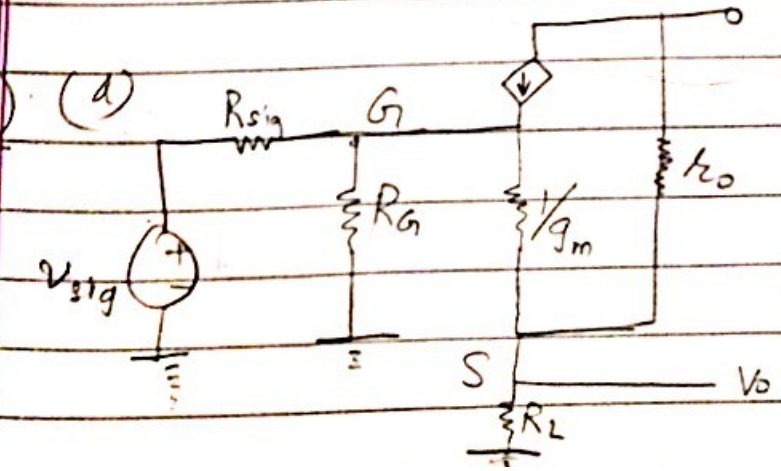
$\Rightarrow V_G = 3\ V$

Now, $\frac{R_2}{R_1 + R_2} \cdot V_{SS} = 3V$

$\frac{R_2}{R_1 + R_2}$ → 1

$\Rightarrow R_2 = 0.3\ \Omega$

Q.3) (a)



(b) $G_V = \frac{v_o}{v_{sig}}$

Microelectronic Circuits Notes Akshansh

(b) $V_i = V_{sig} \times \frac{R_{in}}{R_{in} + R_{sig}}$ $\left(R_{in} = R_G\right)$

$$\frac{V_i}{V_{sig}} = \frac{R_G}{R_G + R_{sig}} \rightarrow (1)$$

We know, $G_V = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \times \frac{V_i}{V_{sig}} = A_V \times \frac{V_i}{V_{sig}}$

$\frac{V_o}{V_i}$ = Voltage gain, $A_V = \frac{R_L // r_o}{R_L // r_o + 1/g_m} \rightarrow (2)$

$$\Rightarrow G_V = \left(\frac{R_L // r_o}{R_L // r_o + 1/g_m}\right) \frac{R_G}{R_G + R_{sig}}$$

(c) Now,

$A_{Vo} = \frac{r_o}{r_o + 1/g_m} \simeq 1\ V/V$ given

$R_{out} = 1/g_m // r_o \simeq 0.2\ \Omega$ given

Now,

$A_V = \frac{R_L // r_o}{R_L // r_o + 1/g_m} \simeq 0.8746\ V/V$ given

PRACTICE.

Q BJT works as an amplifier. Justify how does it work.

Q. $I_C = 2mA$, $g_m = 2.5\ mA/V$. $g_m = \frac{I_C}{\beta} \Rightarrow \beta = 0.8$

$\beta = 0.8$

$\alpha =$ $\alpha = \frac{\beta}{1+\beta} = \frac{0.8}{1.8}$

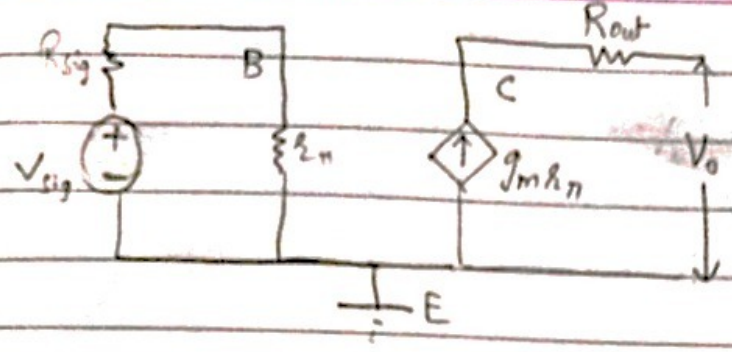
Microelectronic Circuits Notes - Akshansh

Home Assign.

C_2 & R_2 → Find

- C_{C1} ✓ → C_{C2} & C_S → ∞
- C_{C2} ✓ → C_{C1} & C_S → ∞
- C_S ✓ → C_{C1} & C_{C2} → ∞

fig → high pass circuit.



with explanation

Q. Determine mid band gain, upper 3 dB frequency of a CS (Common source) amp. fed with a signal source, having internal resistance of 100 kΩ

Assume: $R_G' = 4.7\ M\Omega$

$R_D = R_L = 15\ k\Omega$

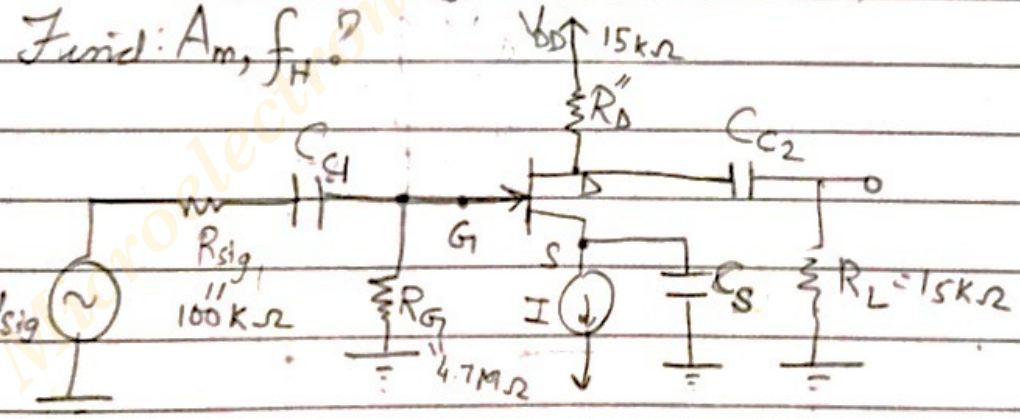
$g_m = 1\ mA/V$

$C_{gs} = 1\ pF$

$C_{gd} = 0.4\ pF$

$r_o = 150\ k\Omega$

Find: A_m, f_H ?



$$A_M = -\frac{R_G}{R_G + R_{sig}} \times g_m \left(R_L'\right)$$

$R_L' = r_o \,//\, R_D \,//\, R_L$

$$= (9.96 \times 10^{-4})(10^{-3})(7.14 \times 10^{3})$$

$$\Rightarrow A_M = 7.1114 \quad V/V$$

$$\text{Gain} = 20 \log(A_M) = 16.90 \text{ dB}$$

Microelectronic Circuits Notes - Akshansh

$R_{sig} // R_g = \frac{(4.7)(0.1)}{(4.8)}$ MΩ = $\simeq 0.979$ MΩ

Puffin Date Page

$$f_H = \frac{1}{2\pi C_{in}(R_{sig} // R_G)} = 38.2 \text{ kHz}$$

$$C_{in} = C_{gs} + \underbrace{(1 + g_m R_L')}_{\text{Miller}} C_{gd}$$

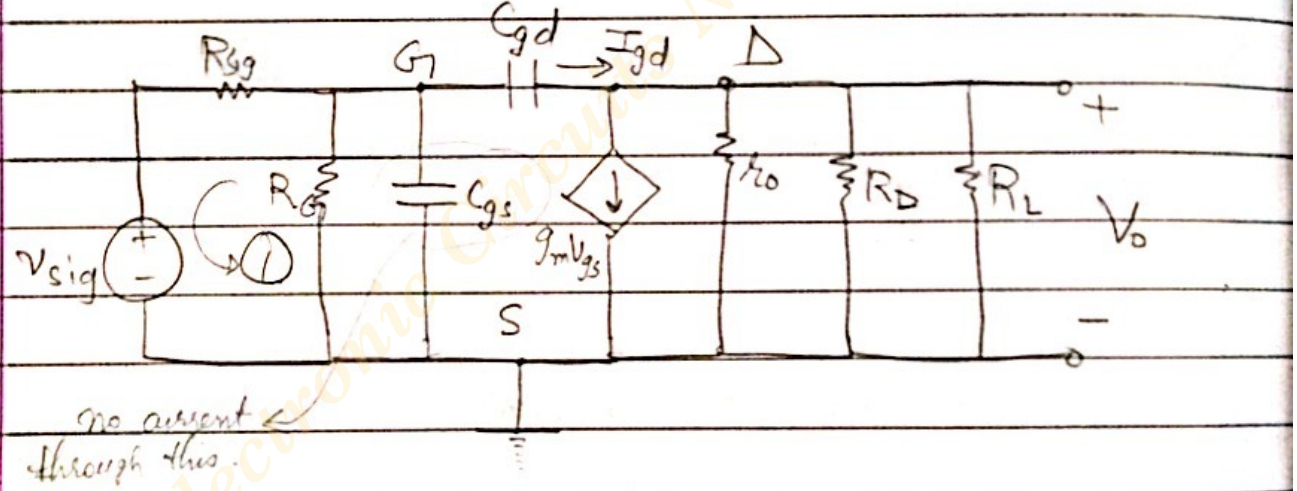
C_{in}

$\Rightarrow C_{in} = 4.256$ pF

(↓ Theory behind above question ↓)

✱ COMMON SOURCE AMPLIFIER

↳ High Frequency Analysis



$$V_o = -g_m V_{gs} (r_o // R_D // R_L)$$

$$\Rightarrow V_o = -(g_m V_{gs})(R_L') \quad ; R_L' = r_o // R_D // R_L$$

$$V_{gs} = \frac{V_{sig}}{R_{sig} + R_G} \times R_G$$ (Voltage divider rule in loop ①)

$$A_M = \frac{V_o}{V_{sig}}$$

Microelectronic Circuits Notes - Ashansh

Q contd.

For some circuit, it is req to choose values of C_{C_1}, C_{eq} & C_S so that amplifier has a lower cut off frequency 100 Hz & that the nearest frequency is atleast a decade later

$$f_L = 100\,KHz$$

done using POS : Consider C_{C_1} → short others
Find C_{eq} & R_{eq}
Consider C_{C_2} → short others
C_{eq} R_{eq} ?
C_S ✓ → short others
C_{eq}, R_{eq} ?

★ Deriving formula for f_H

$TP = 2\pi R_{eq} C_{eq}$

↳ when $v_{sig} = 0$; $R_{eq} = R_G \parallel R_{sig}$

$C = \frac{Q}{V}$

$= \frac{I}{}$

$I = C\frac{V}{t}$

Now, let $R_G \parallel R_D \parallel R_L = R_L'$

We know

$$I = \frac{V}{R} \equiv \frac{V}{X_C}$$

for I_{gd} , $I_{gd} = \frac{V_{gs} - V_o}{X_c} = \frac{V_{gs} - V_o}{\frac{1}{sC_{gd}}}$ → recent pg

$$\Rightarrow I_{gd} = (sC_{gd})(V_{gs} - V_o)$$

Microelectronic Circuits Notes - Arshansh

✡ OLD KNOWLEDGE

* In practical, a capacitor should have leads



These leads will have some resistance.
So, as done before, X_C is what we knew
Taking real case, (lead), so,

Capacitive ~~react~~ reactance, or,
total resistance = $R + jX_C$

So, $X_C = \frac{1}{j\omega C}$ & Ily, $X_L = j\omega L$.

Now, $s = \sigma + j\omega$.
or $s = j\omega$

$\Rightarrow X_C = \frac{1}{sC}$ & $X_L = sL$.

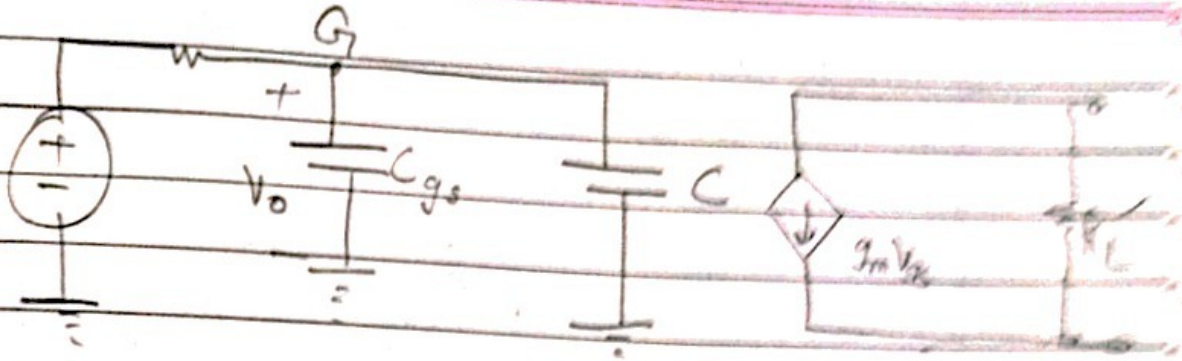
prev. pg · continued

$\Rightarrow I_{gd} = sC_{gd}\left[V_{gs} - (-g_m R_L' V_{gs})\right]$

$-g_m R_L' V_{gs} \rightarrow V_o$ (by KVL) (See fig)

$\Rightarrow I_{gd} = sC_{gd}\left[V_{gs}(1 + g_m R_L')\right]$.

Microelectronic Circuits Notes Akshash



The above circuit knows existence of C_{gd} only through the current I_{gd}

So, we ~~can~~ can replace C_{gd} with C_{eq} b/w gate & GND as long as C_{eq} draws a current equal to I_{gd}.

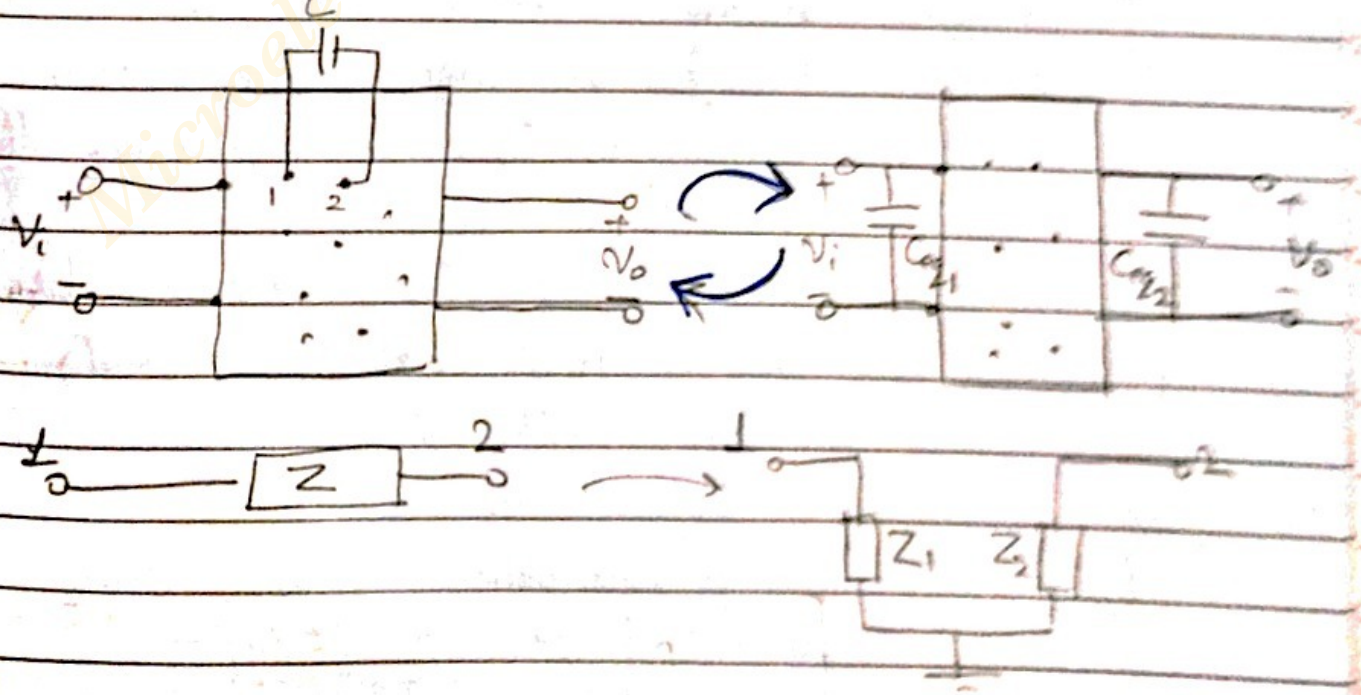
Read through

MILLER'S Theorem:

Consider any sys having NODES

If ∃ a capacitor b/w any 2 nodes, then, that can be represented as a combin^n of 2 capacitors, one at i/p, & other at o/p.

(Electrical equivalent)



Microelectronic Circuits Notes - Akshansh

CIRCUIT

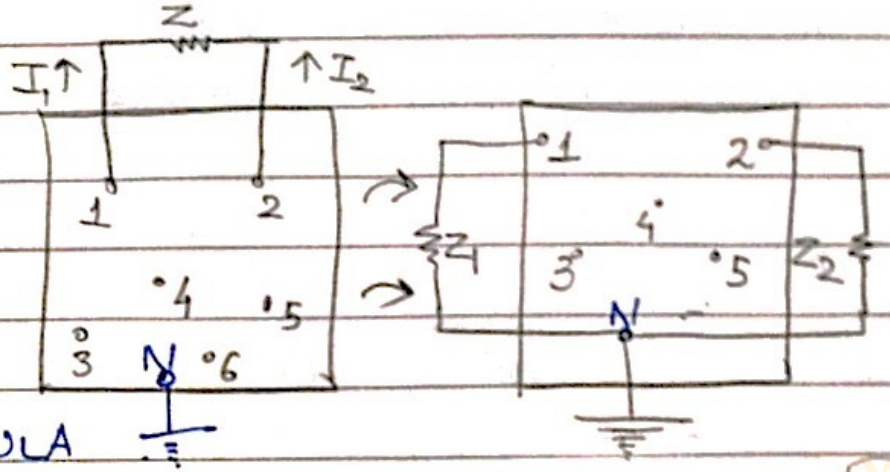


fig (1)

FORMULA

$$Z_1 = \frac{Z}{1-K} \quad , \quad Z_2 = \frac{Z}{1-1/K}$$

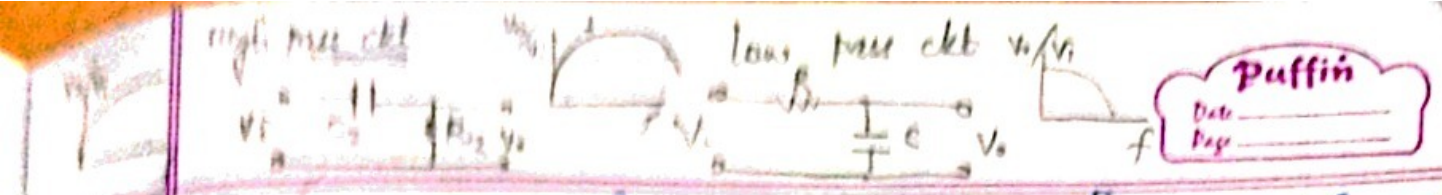
$$\hookrightarrow K = \frac{V_2}{V_1} \quad ; \quad I_2 = -I_1$$

Proof in book

- Integrated Electronics by Jacob Milman
- Van Valkenburg's Network Analysis and Network Synthesis

Defin^n of MILLER's Theorem :- Consider the circuit shown in fig (1). It has n distinct nodes, as shown. & Let the node voltages be termed as $V_1, V_2, V_3, \ldots V_n$, where N is the reference/ground node. Nodes 1 & 2, referred as N_1 & N_2 are interconnected with impedance Z. If we know the ratio, V_2/V_1, (designated as k), & that the current I_1 drawn ~~from through~~ from N_1 through Z & ~~I_2 shown~~ can be obtained by disconnecting terminal 1 from Z & by bridging an impedance, $\frac{Z}{1-k}$ from N_1 to GND

Microelectronic Circuits Notes - Akshansh



Illy, I_2 is drawn from N_2 through Z_k, can be obtained by disconnecting terminal 2 from Z & by bridging $\frac{Z_k}{k-1} = \frac{Z}{1-Y_k}$ impedance from N_2 to GND.

Now, $I_1 = \frac{V_1 - V_2}{Z} = \frac{V_1(1-K)}{Z}$ $\left(\because K = \frac{V_2}{V_1} \text{ assumed}\right)$

$= \frac{V_1}{Z/1-K} = \frac{V}{Z_1}$

PASSIVE Component:

A passive component is one which only dissipates energy within itself. It'll not help in any manner to grow energy & thus, supply an o/p > i/p.

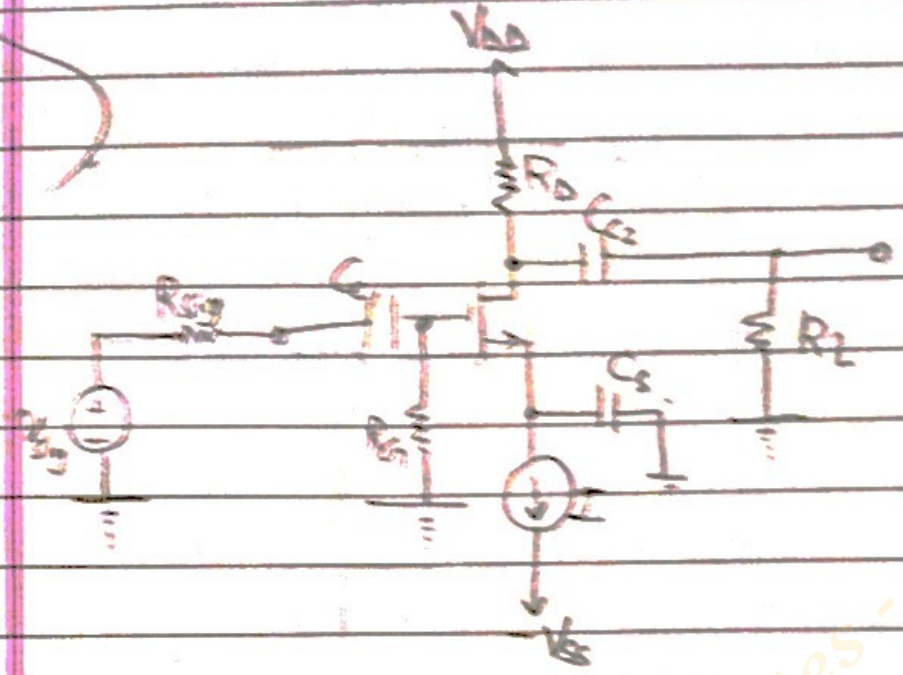
* ⇒ no enhancement of energy (& hence power)
So, if i/p power ≥ o/p power
or i/p energy ≥ o/p energy
⇒ The component is Passive ⇐

• Resistor, transistor, capacitor, Inductor are all passive components.

Illy, if energy (or power) at o/p > i/p energy (or power)
⇒ component is Active.

FREQUENCY RESPONSE

COMMON SOURCE Amp



Earlier assumptions :-

C_{gs}, C_{gd} : Internal capacitors :- DC

C_{C1}, C_{C2}, C_S :- SC

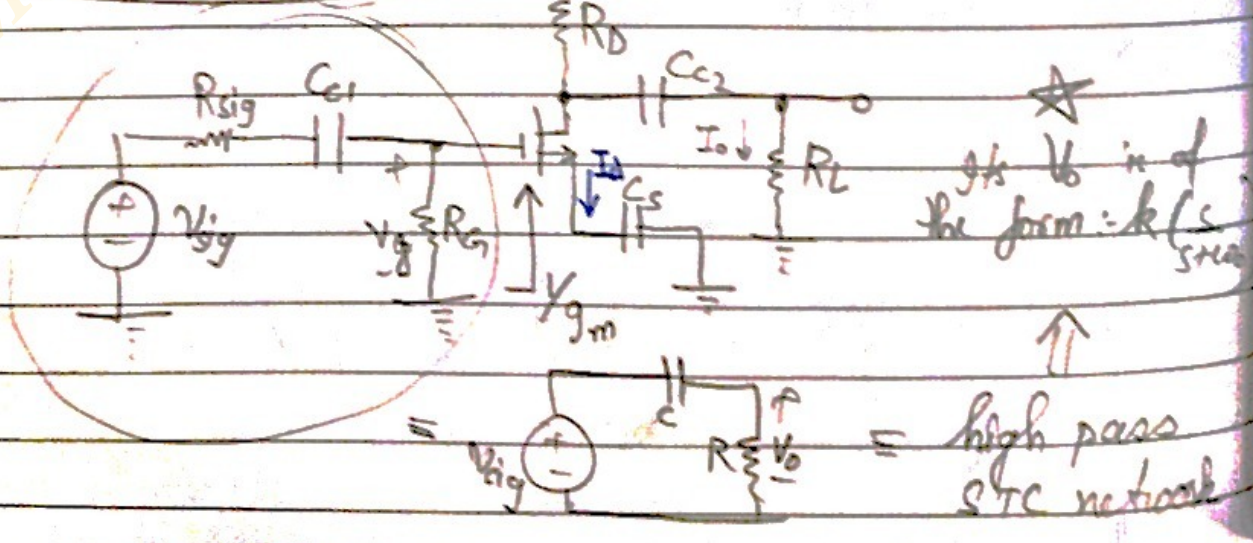
Now, we want to take the effect of frequency

At **LOW FREQUENCY RESPONSE**

↳ S1) Eliminate all DC sources

We are left with the circuit

S2) Considering C_{C1}



☆ its V_o in of the form : $k\left(\frac{s}{s+\omega}\right)$

⇑

= high pass STC network

Microelectronic Circuits Notes - Akshansh

Now, by voltage divider rule,

$$V_g = V_{sig} \times \frac{R_G}{R_G + R_{sig} + \frac{1}{sC_{C1}}}$$

$$= V_{sig} \times R_G \times \frac{s}{sR_G + sR_{sig} + \frac{1}{C_{C1}}}$$

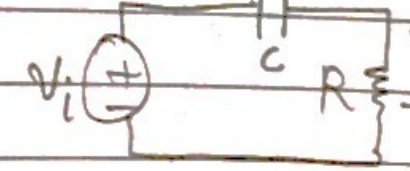
$$= V_{sig} \times R_G \times \frac{s}{s(R_G + R_{sig}) + \frac{1}{C_{C1}}}$$

$$\Rightarrow V_g = V_{sig} \times \frac{R_G}{R_G + R_{sig}} \times \frac{s}{s + \frac{1}{(R_G + R_{sig})C_{C1}}} \rightarrow (1)$$

↳ $s : j\omega$

↳ comes from high pass STC network's TF.

↳ Given a high pass STC network as :-



$$\Rightarrow V_o = V_i \left(\frac{R}{R + 1/sC} \right)$$

$$= V_i R \left(\frac{s}{s + \frac{1}{RC}} \right)$$

$$\Rightarrow V_o = V_i R \left(\frac{s}{s + \omega_0} \right)$$

ω_0 : break frequency of this high pass STC network.

Microelectronic Circuits Notes - Akshansh

Comparing eq^n (1) with std form of high pass STC network

$$\Rightarrow \omega_0 = \frac{1}{(R_G + R_{sig}) C_{c1}}$$

$$\omega_0 = 2\pi f_{P1} = \frac{1}{(R_G + R_{sig}) C_{c1}}$$

break frequency for 1st capacitor $\rightarrow C_{c1}$

$$\Rightarrow \boxed{f_{P1} = \frac{1}{2\pi (R_G + R_{sig}) C_{c1}}}$$

S3) Now, Considering C_s

$$I_d = \frac{V_g}{\frac{1}{g_m} + \frac{1}{sC_s}} \quad \text{(ohm's law)}$$

$$= V_g \left(\frac{s g_m C_s}{sC_s + g_m} \right)$$

$$= V_g g_m \left(\frac{sC_s}{sC_s + g_m} \right)$$

$$= V_g g_m \frac{s}{\left(s + \frac{g_m}{C_s}\right)} \equiv k \left(\frac{s}{s + \omega_0} \right)$$

$$\Rightarrow \omega_0 = \frac{g_m}{C_s}$$

$$\Rightarrow \boxed{f_{P2} = \frac{\omega}{2\pi f} = \frac{1}{2\pi} \frac{g_m}{C_s}}$$

Microelectronic Circuits Notes - Akshansh

54) Considering C_{C2}

$V_o = I_o R_L$

$\hookrightarrow I_o = I_d \times \left[\frac{R_D}{R_D + R_L + \frac{1}{sC_{C2}}}\right]$ (Current divider rule)

$\Rightarrow I_o = I_d \times \left(\frac{R_D}{R_D + R_L}\right) \times \frac{s}{\left[s + \frac{1}{C_{C2}(R_D + R_L)}\right]}$

$\Rightarrow V_o = \frac{I_d R_D R_L}{R_D + R_L} \left[\frac{s}{s + \frac{1}{C_{C2}(R_D + R_L)}}\right]$

$= K\left(\frac{s}{s + \omega_0}\right)$

So, $\omega_0 = \frac{1}{(R_D + R_L) C_{C2}}$

$\Rightarrow \boxed{f_{P3} = \frac{1}{2\pi}\left(\frac{1}{(R_D + R_L) C_{C2}}\right)}$

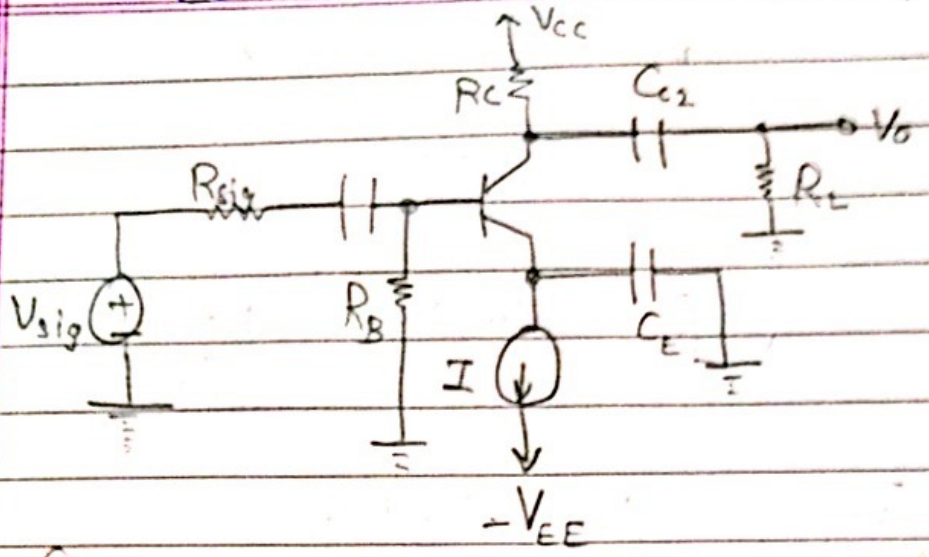
Out of f_{P1}, f_{P2}, f_{P3}; f_{P2} is smallest

So, $f_{P2} \approx f_L$ = lower 3 dB frequency.

f_{P1} & f_{P3} are generally 4 to 5 times greater than f_{P2}.

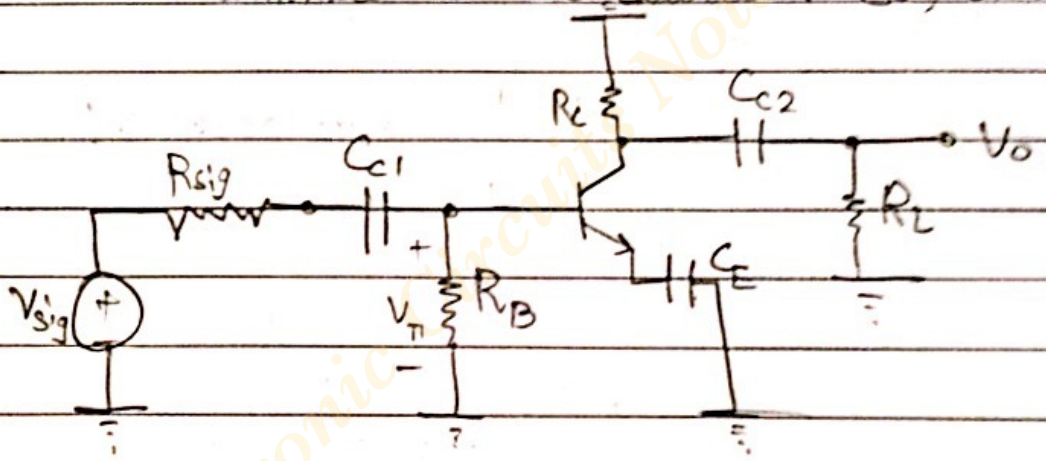
Microelectronic Circuits Notes - Akshansh

FREQUENCY RESPONSE
COMMON EMITTER Amp.

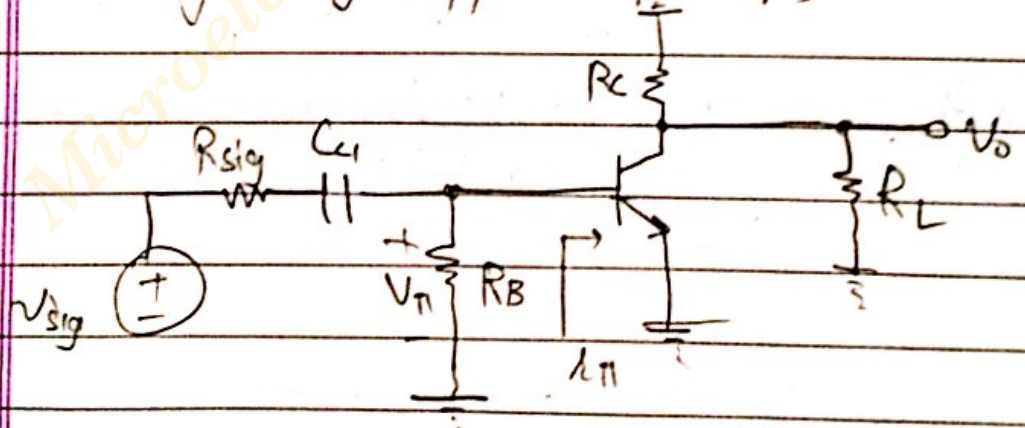


for LOW FREQUENCY RESPONSE

S1) Eliminate all DC sources. So, ckt →



S2) Seeing only effect of C_{c1},



Now, $V_\pi = (V_{sig}) \left[\dfrac{R_B \parallel h_\pi}{R_{sig} + R_B + \dfrac{1}{sC_{c1}}} \right]$

Microelectronic Circuit Notes - Akshansh

Puffin
Date
Page

& , $V_o = -g_m V_\pi (R_C \| R_L)$

↳ comes from hybrid-π model of BJT.

$\Rightarrow V_o = (-g_m)\left[(V_{sig}) \times \frac{(R_B \| r_\pi)}{R_{sig} + R_B \| r_\pi + \frac{1}{sC_{C_1}}}\right](R_C \| R_L)$

$\Rightarrow \frac{V_o}{V_{sig}} = (-g_m)\left(\frac{R_B \| r_\pi}{R_{sig} + R_B \| r_\pi + \frac{1}{sC_{C_1}}}\right)(R_C \| R_L)$

Again, it should be of the form, $k \cdot \frac{s}{s+\omega_0}$

[∵ the circuit resembles a high pass STC network, whose TF is of the form $\left(k \cdot \frac{s}{s+\omega_0}\right)$]

$\omega_{P1} = \frac{1}{RC}$

↳ C_{C_1} here

Resistance seen b/w $C_{C_1} = R_B \| r_\pi + R_{sig}$

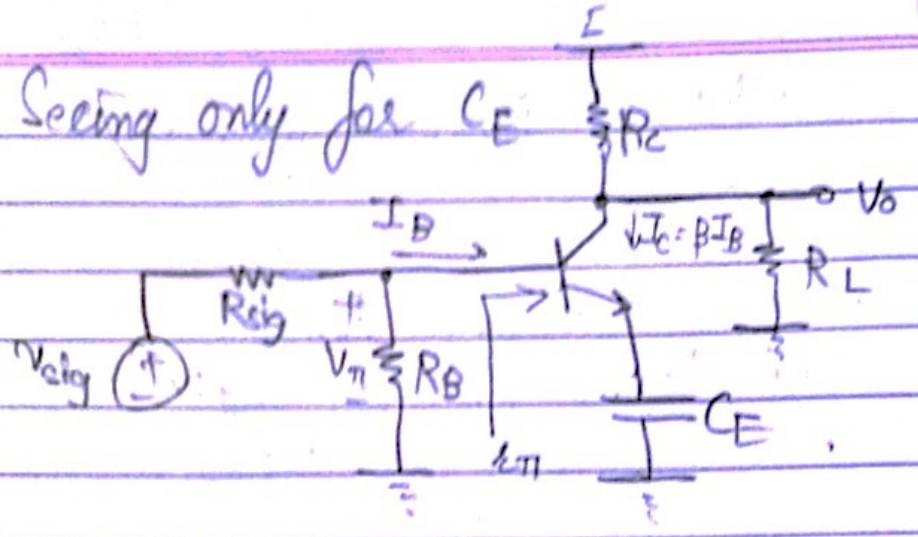
$\Rightarrow \frac{V_o}{V_{sig}} = \underbrace{-g_m\left[\frac{(R_B \| r_\pi)(R_C \| R_L)}{(R_{sig} + R_B \| r_\pi)}\right]}_{k} \times \left[\frac{s}{s + \frac{1}{(R_{sig} + R_B \| r_\pi) C_{C_1}}}\right]$

$\Rightarrow \omega_{P1} = \frac{1}{(R_{sig} + R_B \| r_\pi) C_{C_1}}$

$\Rightarrow f_{P1} = \left(\frac{1}{2\pi}\right)\left(\frac{1}{(R_{sig} + R_B \| r_\pi) C_{C_1}}\right)$

Microelectronic Circuits - Nitish Arishanti

S3) Seeing only for C_E



$V_o = -\beta I_B (R_C \| R_L)$ → written by making equivalent circuit (Hybrid - π) on o/p side

↳ (1)

Resistance in emitter side = $r_e + \frac{1}{sC_E}$

↳ Transfer to base

$\Rightarrow (1+\beta)\left(r_e + \frac{1}{sC_E}\right) = R$

$\Rightarrow I_B = \frac{V_\pi}{R}$

$= \left[V_{sig}\left(\frac{R_B}{R_B + R_{sig}}\right)\right]\left[\frac{1}{R}\right]$

$\Rightarrow I_B = \left(V_{sig}\right)\left(\frac{R_B}{R_B + R_{sig}}\right)\left[\frac{1}{(1+\beta)\left(r_e + \frac{1}{sC_E}\right) + R_B \| R_{sig}}\right]$

↳ (2)

Using (2) in (1)

$\Rightarrow V_o = (-\beta)\left[V_{sig} * \left(\frac{R_B}{R_B + R_{sig}}\right) * \frac{R_C \| R_L}{(1+\beta)\left(r_e + \frac{1}{sC_E}\right) + R_B \| R_{sig}}\right]$

Microelectronic Circuits Notes by Ishansh

$$\Rightarrow \frac{V_o}{V_{sig}} = -\beta \frac{R_B}{R_B + R_{sig}} \times \frac{R_C // R_L}{(1+\beta)\left(r_e + \frac{1}{sC_E}\right) + R_B // R_{sig}}$$

$$= \left(-\beta \frac{R_B}{R_B + R_{sig}} \times R_C // R_L\right) \left[\frac{s}{s\left[R_B // R_{sig} + r_e(1+\beta)\right] + \frac{1+\beta}{C_E}}\right]$$

$$= \underbrace{\left(-\beta \frac{R_B}{R_B + R_{sig}} \times R_C // R_L\right) \left[\frac{1}{R_B // R_{sig} + r_e(1+\beta)}\right]}_{k} \left[\frac{s}{s + \frac{1+\beta}{C_E(R_B // R_{sig} + r_e(1+\beta))}}\right]$$

$$= k\left(\frac{s}{s + \frac{1}{C_E\left(\frac{R_B // R_{sig}}{1+\beta} + r_e\right)}}\right)$$

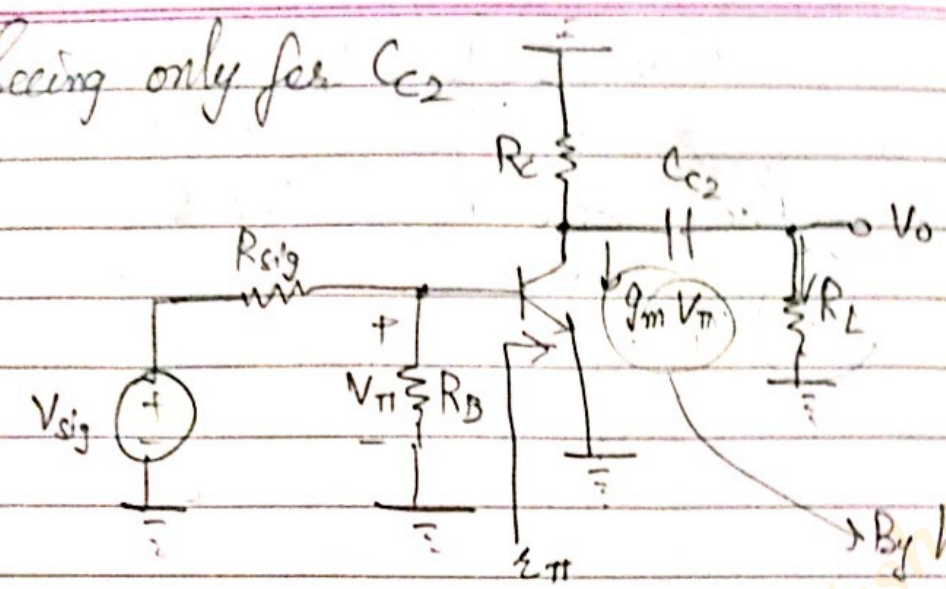
$$k \cdot \frac{s}{s + \omega_{p_2}}$$

$$\Rightarrow \omega_{p_2} = \frac{1}{C_E\left(\frac{R_B // R_{sig}}{(1+\beta)} + r_e\right)}$$

$$\Rightarrow f_{p_2} = \left(\frac{1}{2\pi}\right)\left(\frac{1}{C_E\left(\frac{R_B // R_{sig}}{(1+\beta)} + r_e\right)}\right)$$

Microelectronic Circuits Notes - Akshansh

(S4) Seeing only for C_{C2}



① $V_o = \left[-g_m V_\pi \left(\frac{R_C}{R_C + \left(R_L + \frac{1}{sC_{C2}}\right)} \right) \right] \times R_L$

② $V_\pi = V_{sig} \times \left(\frac{R_B // r_\pi}{R_{sig} + R_B // r_\pi} \right)$ → by current divider rule.

Using ② in ①.

$$\Rightarrow \frac{V_o}{V_{sig}} = -g_m \left(\frac{R_B // r_\pi}{R_B // r_\pi + R_{sig}} \right) \left(\frac{R_C R_L}{\left(R_C + R_L + \frac{1}{sC_{C2}}\right)} \right)$$

$$= \underbrace{\left[-g_m \frac{(R_B // r_\pi)(R_C R_L)}{(R_B // r_\pi + R_{sig})(R_C + R_L)} \right]}_{k} \left[\frac{s}{s + \frac{1}{(R_C + R_L) C_{C2}}} \right]$$

k ///

$k \cdot \frac{s}{s + \omega_0}$

$$\Rightarrow \omega_{P3} = \frac{1}{(R_C + R_L) C_{C2}}$$

$$\Rightarrow f_{P3} = \left(\frac{1}{2\pi}\right) \left(\frac{1}{(R_C + R_L) C_{C2}} \right)$$

Microelectronic Circuits Notes - Akshansh

S5) Considering effect of f_{P1}, f_{P2} & f_{P3}

$$\frac{V_o}{V_{sig}} = A_M \left(\frac{s}{s+\omega_{P1}}\right)\left(\frac{s}{s+\omega_{P2}}\right)\left(\frac{s}{s+\omega_{P3}}\right)$$

↳ find A_M

then, $f_L = \frac{A_M}{\sqrt{2}}$ ✓

TUTORIAL

Q Perform :-

(a) Small signal analysis of MOS Cascode

(b) Frequency response analysis of MOS Cascode

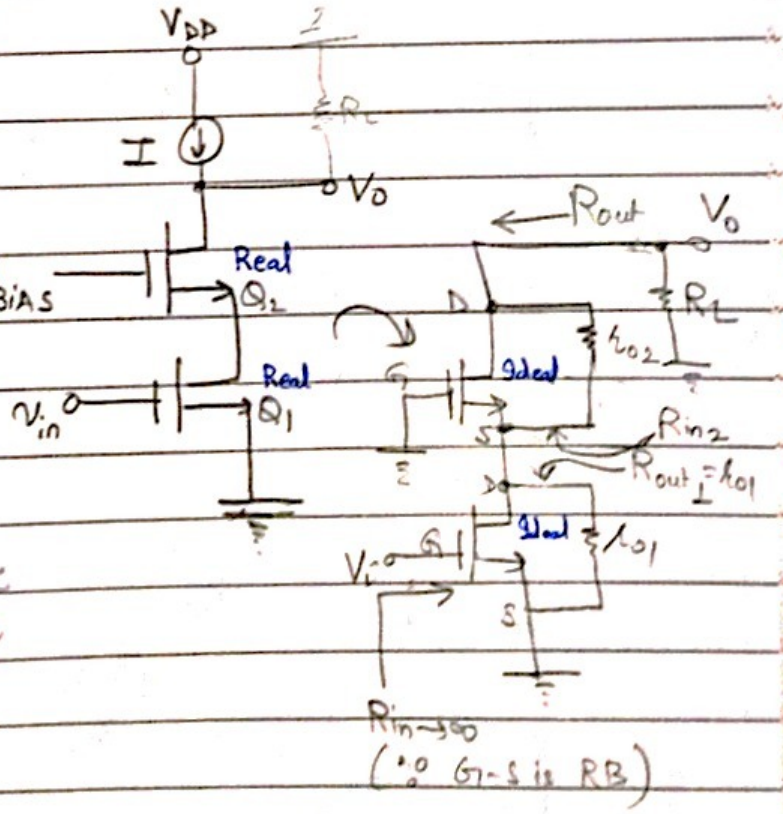
(a) for small signal analysis

S1) recall small signal device model

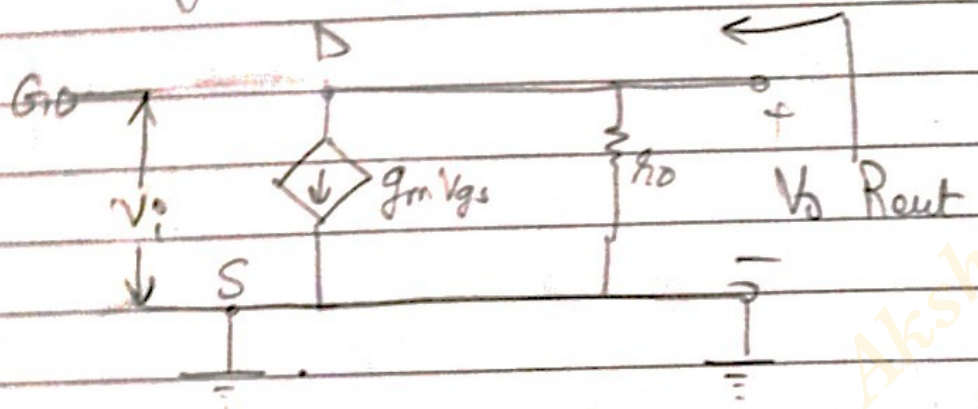
S2) Draw equivalent ckt

↳ Idea :-

DC Sources: Voltage source : sc; Current source : oc



Small signal hybrid-π model



See the model for →

Q1 : CS MOS

Q2 : CG MOS.

$R_{in} \rightarrow \infty$

$R_{out_1} = r_{o1}$

$R_{in_2} = \frac{1}{g_{m2} + g_{m1}}$

$R_{out} = \frac{R_L}{A_{vo2}}$

* Each capacitance present in any model corresponds to one break frequency.

Microelectronic Circuits Notes - Akshansh

Date 21/4/13
Day

Ch-8

MULTISTAGE AMPLIFIERS

benefits: { ✓ Improved / higher gain
✓ Design flexibility & versatility

* For delivering max. (i/p) at Ri

i.e. for current source : $R_s \to \infty$, $R_i \to 0$
voltage source : $R_s \to 0$, $R_i \to \infty$

• while designing an amplifier, we need,
- 4 resistors
- 3 capacitors
- 1 power supply
- 1 BJT/FET

} all of them have to satisfy the values of R_{in}, R_{out}, f_L & f_H in one SINGLE STAGE

So, multistage amplifiers are used

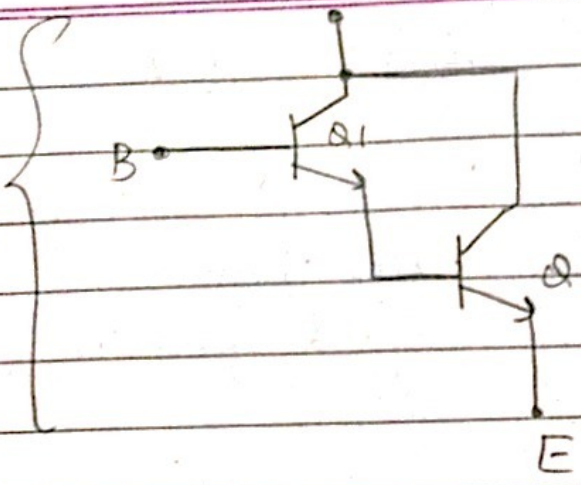
1st stage
looks after coupling (i/p) → voltage/current/power

2nd stage
Bulk gain taken care of → mid band gain

3rd stage
used to connect multiple devices
• looks after (o/p) coupling → voltage/current/power

If we need higher mid band gain, put one more stage in between ⇒ Total 4 stages (2nd & 3rd stage take care of bulk gain)

Electronic Circuits Notes - Abhiansh



* Compound device

Both Q_1 & Q_2 will be exposed to same envt.
Any change in 1 ⇒ Change in other
↳ in parameters, temp, ---

No change in parameter ⇓ characteristics remain the same ⇓ Drifts from their values reduces ⇓ Stability ↑

- Compound devices such as Darlington pair, totempole config., boot strap config., cascade config., are a motivation for multistage amp. design, since they possess special characteristics in terms of R_{in}, R_{out}, A_v, A_i, A_p, ——

- When a bounded i/p produces a bounded o/p : sys is stable.
Bounded i/p produces an unbounded o/p : sys is unstable.

* Q Analysis : STABILITY ANALYSIS
↳ needs to be performed in multi-stage amps. so that the amplifier works correctly at ∃ no deviation in its properties.

Microelectronic Circuits Notes - Lakshmish

Puffin
Date
Page



for voltage at o/p of amplifier,
for it to be be max, R_o → should be min
current at o/p, for it to be max, R_o → should be max

* Capacitance (Internal) for BJT

(FB) Diffusion capacitance (C_{BE})

(RB) Transistion capacitance (C_{BC})

* At high frequency : Internal capacitance dominates (External → sc)
Reverse happens for low frequency.

Very imp

Q. Design an amp. using BJT amp (CB or CC or CE or combin^n of them) to have the following specific^{ns} :-

$A_v = 1000$ V/V
$R_{in} = 1\ M\Omega$
$R_{out} = 50\ \Omega$
f_L & f_H (within audio range)
⇓
$f_L = 20$ Hz, $f_H = 20$ kHz

OPEN BOOK Ques. Lil'll be continued in part 2

Q 2N3904 :- NPN General Purpose Amplifier

Current gain → max of 300 (from data sheet) is possible

If $A_v = 1000$, what is A_i

Microelectronic Circuit Notes - Akshansh

Puffin
Date
Page

Max. Power gain possible = 625

$A_P = A_V A_i$

$A_V = \frac{A_P}{A_i} = \frac{625}{300} = \underline{\underline{2.08}}$

$P_{AC\ i/p}$ (ignored (∵ low)) $+ P_{DC\ i/p} = P_{dissipated} + P_{output}$

Operating pt :-

DC Current gain :- $I_c = 10mA$ $V_{CE} = 1.0V$

Gain	Min	Max
	100	300

$P_{dissipated} = V_{CE} I_c = 10mW$

AC Current gain, $h_{fe} = 175$ (from table)

Find Single stage amplifier design

R1, R2, RC, R_E, C_{c1}, C_{c2}, CE

↓

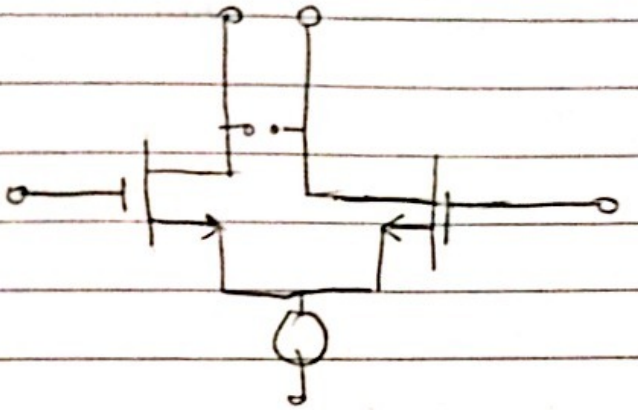
continued after this page →

Microelectronic Circuits Notes - Akshansh

* Source follower amp : CD Amp. } gain = 1
* Emitter follower amp : CC Amp
* DIP : Dual i/p Package
* Differential amp :- Part of op-Amp.

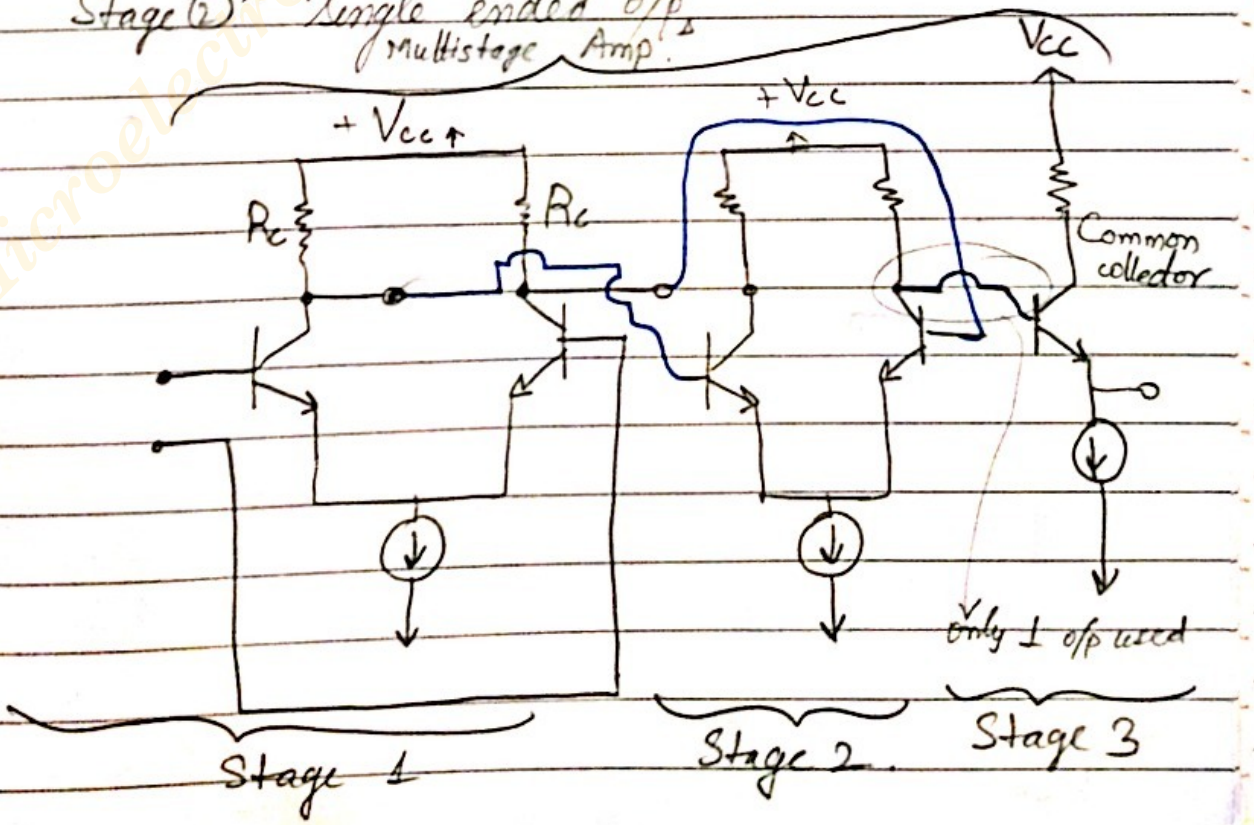
Puffin
Date 25/4/13
Page

☆ Differential Amplifier



* ☆ Op-amp : a differential amp
  : has 2 i/p's → 1 o/p
  * ☆ 2 stage CMOS amp
    └ 1st stage CMOS Op-amp

* ☆ BJT differential amplifier : 2 stages
  Stage ① - Separate o/p's taken from collector
  Stage ② - Single ended o/p



Microelectronic Circuits Notes - Akshansh

Open book ques. → continued

Puffin Date 22/4/18 Page

✱ Designing a multistage amplifier

↳ 1. Specific^{n}.
↳ 2. Possible configur^{ns}.

for our example :- 1) $A_V = 1000$
$R_{in} = 1\,M\Omega$
$R_o = 50\,\Omega$.
f_L & f_H : in audio range
f_L → 20 Hz, f_H → 20 KHz

Idea :- Design an amplifier with above specific^{n} using one/many of :-
- CB/CE/CC : BJT
- CS/CD/CG : FET

• We used BJT → Q2N3904 for that (details of it, in Table no. (3.9))

Idea: We are given $R_{in} = 1\,M\Omega$. So a FET is better (∵ for CS, S & G : RB ⇒ High i/p impedance)
So, making a MOS followed by BJT is possible as:-

Vi → Stage 1 (MOS, CS) → Stage 2 (BJT, CE) → O/p

make it s.t gives gain 5 (or 10) | gain → 200 (or 100) | 5 × 200 = 1000 ✓ (10 × 100 = 1000 ✓)

Microelectronic Circuits Notes: Akshansh

★ Configurations are there in Table 4.4

Idea ② :- Use this config

Identical

Stage ① | Stage ② | Stage ③

MOS | BJT | BJT

(any gain) | Say it gives gain of 35 | 35

35 × 35 = 1225

So, gain > 1000 is got

Idea ③ :- What if we use this config :

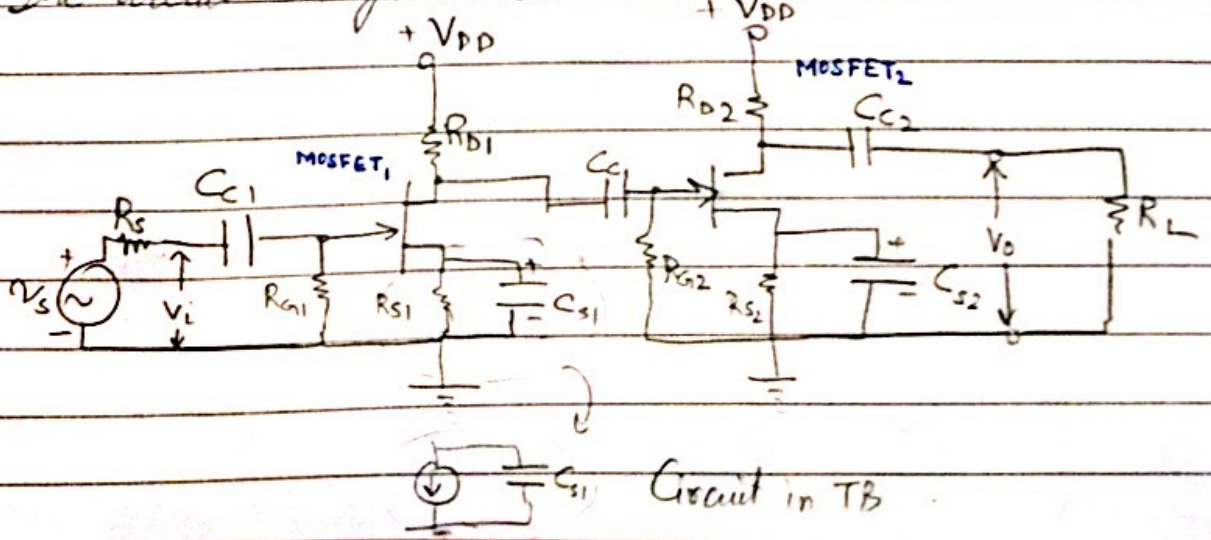
i/p → [MOS] [MOS] → o/p

gain of 35 | gain of 35

1225

Consider idea ③ as an option for the time being :-

The circuit diagram becomes :



C_{S1} Circuit in TB

Microelectronic Circuits Notes by Akshansh

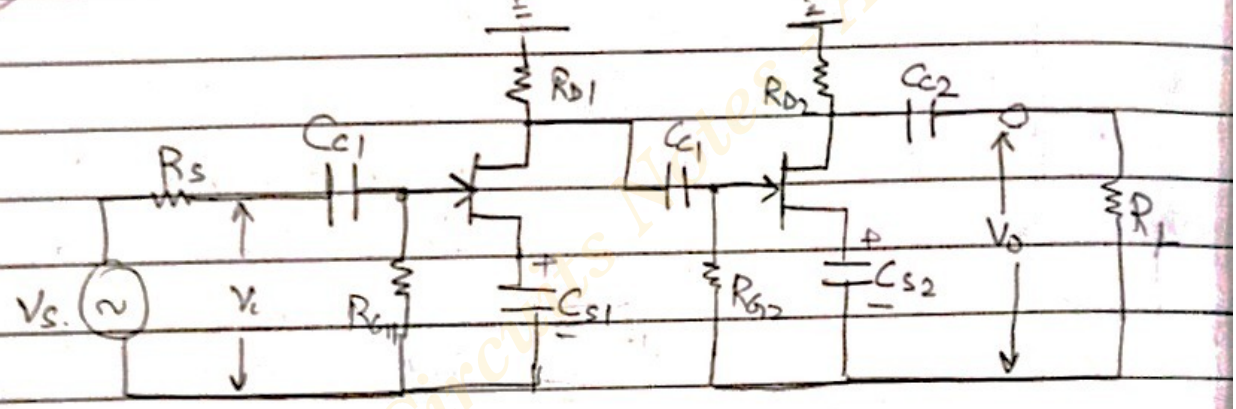
The components in prev. circuit :-

3 Resistors, 3 Capacitors & 3 R_L, 3 C_L & R_L

STAGE ① Stage ②

We need to find their values so as to complete the circuit.

(Way 1) S1) Eliminate all DC sources. So, we have



So, $R_{G1} = R_{in} = 1M\Omega$

$R_{D2} = R_{out} = 50\Omega$

Now, calculate value of

$$g_m = k_n' \frac{W}{L} V_{ov}$$

Set A_{v_0} as 35 for first stage.

$A_v = -g_m(R_L \| r_o)$ $\quad A_{v_{0_1}} = -g_m R_{D1}$

$1 + g_m R_{S1}$

So, $R_{D1}, g_m, A_{v_{01}}$: known

$\downarrow$

R_{S1}

Similarly, for $A_{v_{02}} \rightarrow R_{S2}$

Microelectronic Circuits Nitee Akshansh

Puffin
Date
Page

(Way 2) for MOSFET, we need to bias it. Biasing is done in satur^n region.

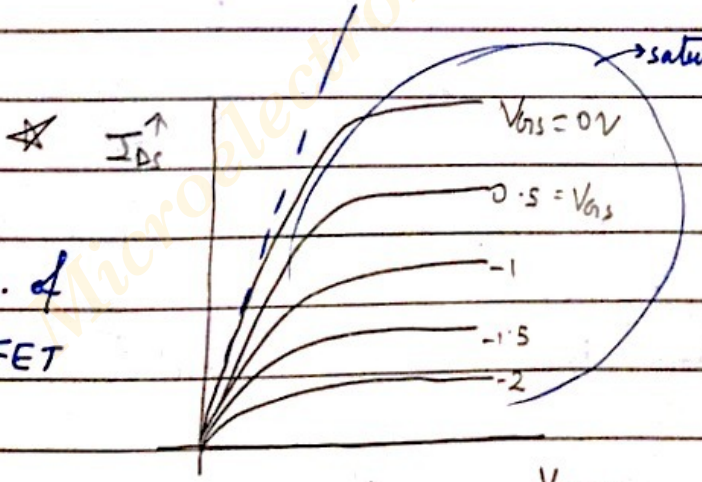
In Way (1), biasing wasn't done. So, state of FET isn't clear.
The operating pt. is necessary to be known for a FET.

So, $(V_{DS})_{1,2}$ & $(I_{DS})_{1,2}$ should be calculated →

See if operating pt is in satur^n region or not

Saturn region: go further

not in satur^n: we won't know whether amplific^n will take place or not



o/p charac. of MOSFET

If we assume our FET in satur^n region, then the value of V_{DS} & I_{DS} should be such that V_{DS}, I_{DS} should lie in satur^n region.

— open book ques. continued after topic of Differential amplifier.

Microelectronic Circuits Notes Akshay

DIFFERENTIAL AMPLIFIER

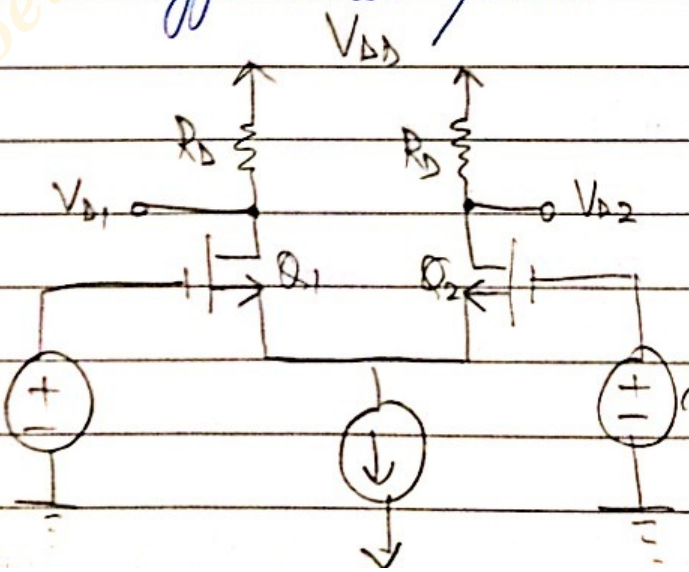
* Operation of transistor in the saturⁿ region :-

$$V_{DS} > V_{GS} - V_{TH}$$

or $V_{DS} > V_{ov}$ → overdrive voltage

* Differential ampl. as compared to single ended :
  - less sensitive to noise & interference
  - Biasing / coupling b/w stages do not require capacitors (like, C_{C1}, C_{C2} & all are not reqd to combine multiple amplifiers)

* MOS Differential pair

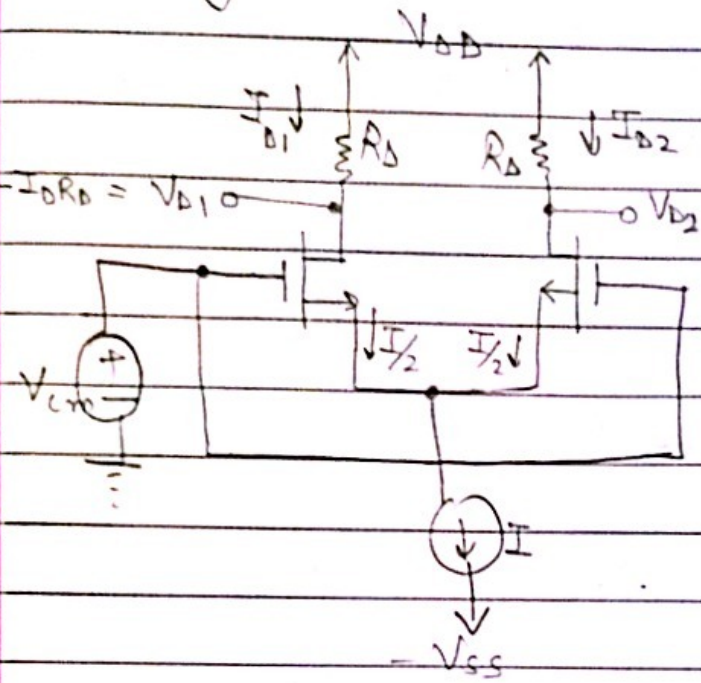


(fig 1)

Microelectronic Circuits Notes Akshansh

$\star$ $k_n' = \mu_n \cdot C_{ox}$

Considering a common mode voltage



2 sides of Differential ampl. → perfectly symmetrical.

Differential pair rejects common mode signals.

↳ ∴ $V_{D1} = V_{D2}$

So, $o/p = V_{D1} - V_{D2} = 0$.

∴ rejection.

OFFSET VOLTAGE (Seen in MOSFET)

Seeing fig 1), sometimes, ∃ o/p even if the i/p's, V_{G1} & V_{G2} are zero.

This voltage is called o/p offset voltage.

It is denoted by V_{OS}

For an o/p offset voltage of V_o, i/p offset voltage is $V_{os} = \frac{V_o}{A_d}$.

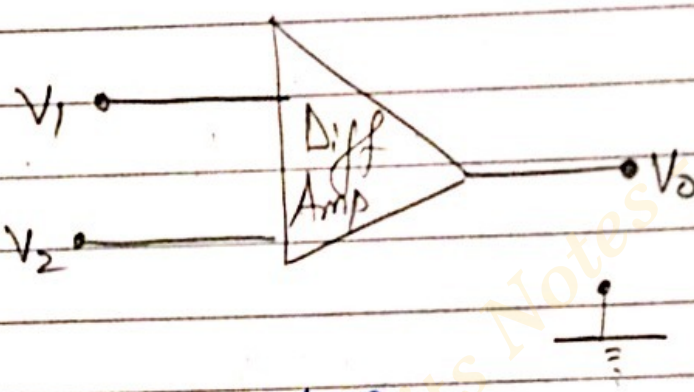
Now, for removing this extra voltage that was coming at o/p (due to fabric^n tech.), then, apply $-V_{os}$ at i/p.

Microelectronic Circuits Notes - Akshansh

Offset voltage (seen in BJT)
- due to mismatch in R_L, Junction area, β & other mismatches in BJT diff. amp.

Imp CMRR in a Differential Stage

Pg 505 → Millman's textbook (Ch-15) : A deriv^n



For an ideal diff. amp,

$$V_o = A_d (V_1 - V_2)$$

For practical case,

$$V_o = A_1 V_1 + A_2 V_2$$

↳ i/p amplific^n from V_1 to V_o keeping V_2 grounded.

* V_d : difference signal b/w i/ps V_1 & $V_2 = V_1 - V_2$
* V_c : avg. value of signal $= \frac{V_1 + V_2}{2}$.

To find CMRR :- $\rho = \frac{A_d}{A_c}$

Microelectronic Circuits Notes Akshansh

Idea: Find CMRR.

So, in the expression:- $V_o = A_1 V_1 + A_2 V_2$, → (1)

by definition ← Find V_o in terms of V_d, V_c, A_d, A_c

Now, $V_d = V_1 - V_2$ ⇒ $V_1 = V_d + V_2$

& $V_c = \frac{V_1 + V_2}{2}$ ⇒ $V_1 + V_2 = 2V_c$

⇒ $V_2 = 2V_c - V_1$

⇒ $V_1 = V_d + (2V_c - V_1)$

⇒ $2V_1 = V_d + 2V_c$

⇒ $V_1 = \frac{V_d}{2} + V_c$ → (2)

Also, Now, $V_2 = V_1 - V_d$

$= (2V_c - V_2) - V_d$

⇒ $2V_2 = 2V_c - V_d$

⇒ $V_2 = V_c - \frac{V_d}{2}$ → (3)

Substituting (2) & (3) in (1) -

⇒ $V_o = A_1\left(\frac{V_d}{2} + V_c\right) + A_2\left(V_c - \frac{V_d}{2}\right)$

⇒ $V_o = V_d\left(\frac{A_1}{2} - \frac{A_2}{2}\right) + V_c(A_1 + A_2)$

Now, A_d = voltage gain for difference signal $= \frac{1}{2}(A_1 - A_2)$

A_c = voltage gain of Avg. signal $= A_1 + A_2$

⇒ $V_o = A_d V_d + A_c V_c$.

Microelectronic Circuits Notes - Akshansh

Now, CMRR, $\rho = \frac{A_d}{A_c}$

So, in $V_o = A_d V_d + A_c V_c$

$$= A_d V_d \left(1 + \frac{A_c}{A_d}\frac{V_c}{V_d}\right)$$

$$\Rightarrow \boxed{V_o = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_c}{V_d}\right)}$$

Q. Let (i) $V_1 = 50\mu V$, $V_2 = -50\mu V$.

(ii) $V_1 = 1050\mu V$, $V_2 = 950\mu V$.

If (a) ρ is 100, find % diff. in o/p voltage obtained for 2 sets of i/p signals

(b) Repeat (a) if $\rho = 10,000$

Now,

$$V_o = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_c}{V_d}\right)$$

Case(i)

$$\Rightarrow V_d = V_1 - V_2 = 100\mu V$$

$$V_c = \frac{V_1 + V_2}{2} = 0$$

$$V_o = 100 A_d$$

Case(ii).

$$V_d = V_1 - V_2 = 100\mu V.$$

$$V_c = \frac{V_1 + V_2}{2} = 1000\mu V.$$

$$V_o = 100 A_d \left(1 + \frac{1}{100}\frac{1000}{100}\right) = 110 A_d$$

Microelectronic Circuits Notes Akshansh

So, ∃ a diff. of 10 % for each set of signal.

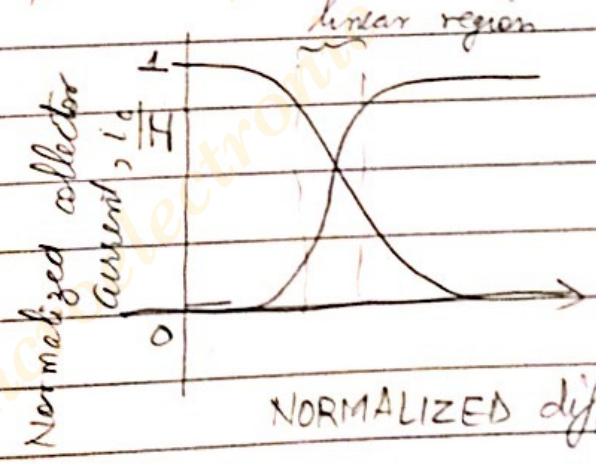
(b) Repeat for β = 10,000.
∃ 0.1 % difference

Ans

✱ TRANSFER Characteristics

↳ Basically, a curve b/w i/p & o/p.

✱ Considering the transfer characteristics of a BJT differential pair:



V_{id} : difference b/w 2 i/p voltages of differential amp

This response can be generalised ∀ BJT, FET or any circuit. ∴ we have NORMALIZED it.

✓ for i/p → $\frac{V_d}{(V_T)}$ → a constt value at RT

Microelectronic Circuits Notes - Akshansh

Puffin

Open book quiz : Continued

- While designing a multistage amplifier with given specifications:

Idea :- Think of :

- Which device : BJT / FET
- How many stages ?
  - 1 / 2 / 3 / 4 . . .
  - 1 : not possible here
  - 2 : it requires multi-stage

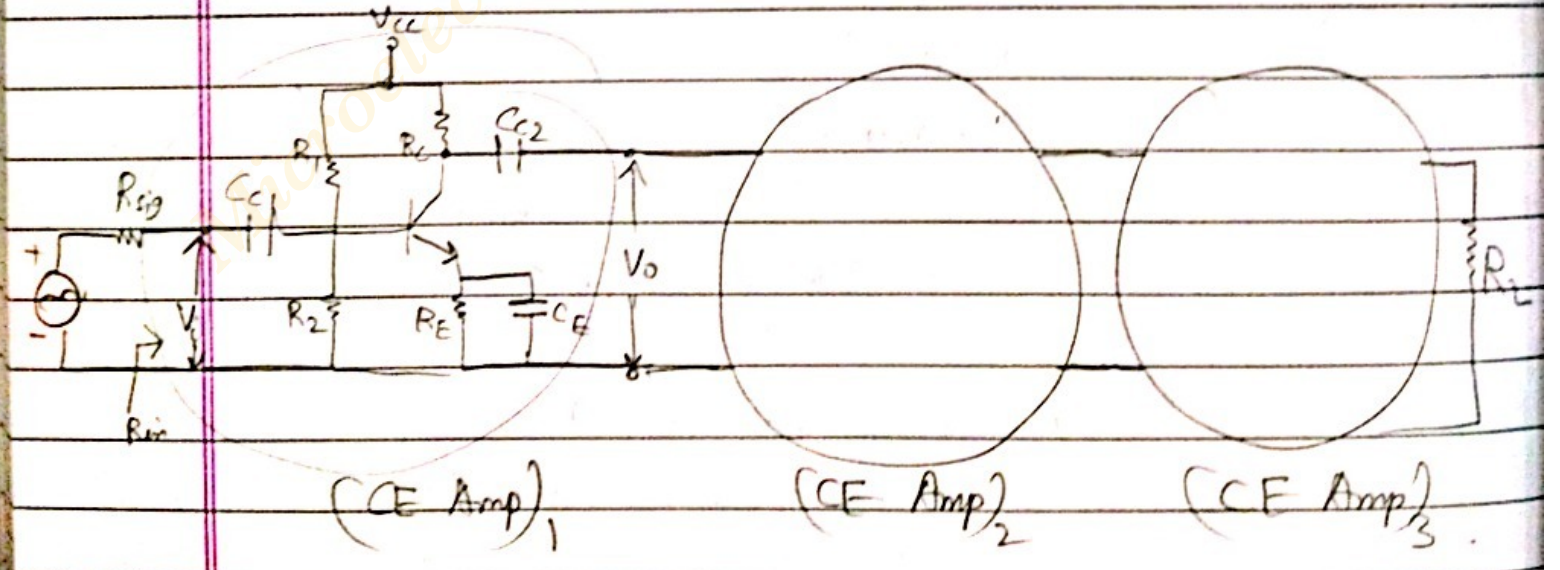
Here, we needed a gain of 1000

So, (Way 1) → Design 3 IDENTICAL Stages

→ gain of 10 in each stage

⇒ Total gain of $10 \times 10 \times 10 = 1000$

Suppose we choose a CE ampl.



Electronic Circuits Notes - Akshesh

Note :- We are amplifying here
So, the BJT/FET used here should be in Active region
↳ EBJ → FB & CBJ → RB

Now,

$$A_{vf} = -\frac{R_D}{R_D + R_{sig}} \times g_m (R_D \| R_L)$$

A_{vf}, for us is 10 dB for each.
So, amplifying it, we have to look into

$$g_m = \frac{I_C}{V_T} = \frac{I_C}{25mV}.$$

Value of I_C → can be got by knowing
* R_1, R_2 & h_E

* $R_B = R_1 \| R_2$

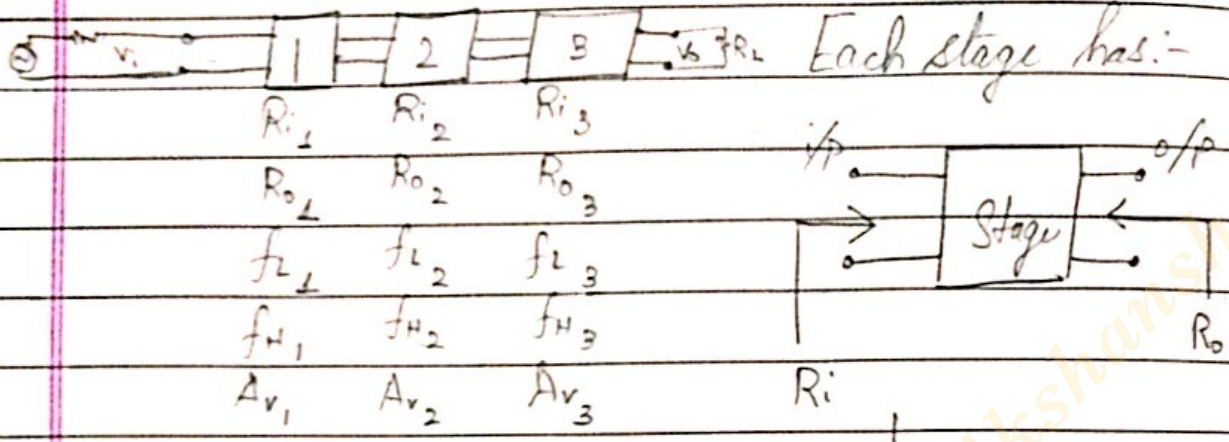
for the voltage (V_{sig}) given from source, we need that same value at V_i.
for that $R_{sig} \longrightarrow 0$. (not physically possible)

Now, R_{in} is in parallel to R_{TH}
Whatever new resistor we connect at i/p it'll be in parallel.
So, we won't get 1 MΩ as R_{in} (as asked in ques)

So, BJT RULED OUT!

Microelectronic Circuits Notes - Akshansh

We are working on the idea:



Each stage has:-

For the overall 3 stages,

$$A_V\Big|_{\text{overall}} = A_{V_1} \times A_{V_2} \times A_{V_3}$$

$$f_L\Big|_{\text{overall}} =$$

$$f_H\Big|_{\text{overall}}$$

finding f_H^* :- overall 3-dB high frequency

Let f_{Hi} be 3-dB frequency for i^{th} stage

where $i = 1, 2, 3, \ldots n$. then

$$\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1+\left(\frac{f_H^*}{f_{H1}}\right)^2}} \cdot \frac{1}{\sqrt{1+\left(\frac{f_H^*}{f_{H2}}\right)^2}} \cdots \frac{1}{\sqrt{1+\left(\frac{f_H^*}{f_{Hi}}\right)^2}} \cdots \frac{1}{\sqrt{1+\left(\frac{f_H^*}{f_{Hn}}\right)^2}}$$

→ (1)

Microelectronic Circuits Notes - Akshansh

If frequencies of each stage are identical

$$\left[\frac{1}{\sqrt{1+\left(\frac{f_H^*}{f_H}\right)^2}}\right]^n = \frac{1}{\sqrt{2}}$$

$$\Rightarrow \boxed{\frac{f_H^*}{f_H} = \sqrt{2^{1/n}-1}} \quad \text{Formulae for Non Interacting Stage}$$

$$\text{Ily, } \frac{f_L^*}{f_L} = \frac{1}{\sqrt{2^{1/n}-1}}$$

$\star$

So, f_L, f_H for individual stage :-

$$- f_H = \frac{20{,}000}{\sqrt{2^{1/3}-1}} = 39.22\ KHz$$

$$- f_L = 20 \times \sqrt{2^{1/3}-1} = 10.19\ Hz$$

Valid only if Stages are NON-INTERACTING.

$\star$ ↳ for us, it should always be non interacting

$\star$ If stage is INTERACTING :-

$$\frac{1}{f_H^*} = 1.1\sqrt{\frac{1}{f_{H_1}^2} + \frac{1}{f_{H_2}^2} + \dots \frac{1}{f_{H_n}^2}}$$

Microelectronic Circuits Notes_Akshansh

here, had we used it

$$\frac{1}{f_H^*} = (1.1)\sqrt{\frac{3}{f_H^2}}$$

$$\Rightarrow \frac{1}{20000} = (1.1)\frac{\sqrt{3}}{f_H}$$

$$\Rightarrow f_H = (20,000)(1.1)\sqrt{3}$$

$$\Rightarrow f_H = 38.105 \text{ KHz}.$$

Now, using value of f_H as 39.22 KHz.
& finding f_H^*

$$f_H^* = 20.58 \text{ KHz}$$

Non-Interacting Stages :-

Stage 3 ✓ shouldn't load Stage 2
Stage 2 " " Stage 1
Stage 1 " " Source

↳ If it loads → Interacting Stages

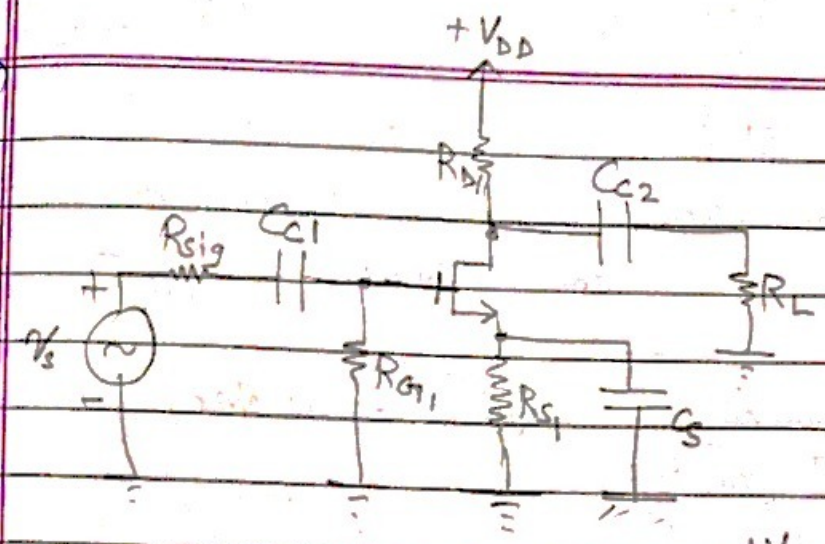
✱ Loading / Non loading :-

Basically decided on seeing that whether entire Source voltage reaches i/p voltage or not
($R_s \to 0$ & $R_{in} >>> R_s$)

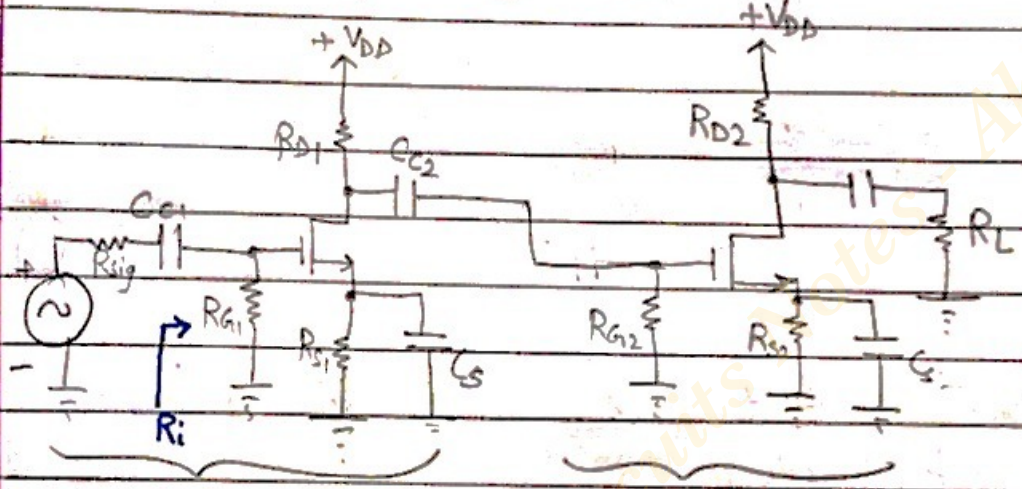
Microelectronic Circuits Notes - Akshansh

* Loading is caused due to voltage division.

Puffin
Date 7/5/2013
Page



: SINGLE STAGE FET Amplifier.



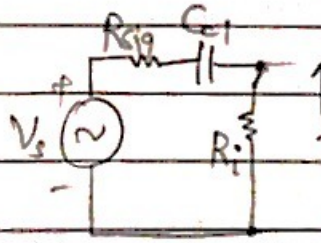
: Cascaded

Stage 1 Stage 2.

↳ for Non-Interacting, R_L shouldn't load stage 2
Stage 2 shouldn't load stage 1

Cond^ns for No loading

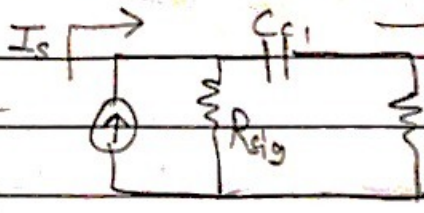
Feed Voltage i/p



$R_{sig} << R_i$

for $V_i = V_s$

Feed current i/p :-



$R_s >> R_i$.

for $I_s = I_i$

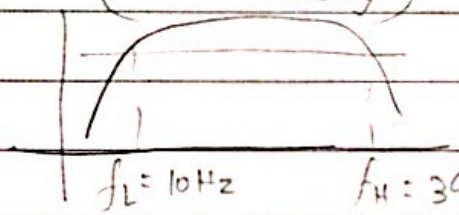
Feed power i/p :- By Max. Power transfer $R_s = R_i$ them,

Power Electronic Circuits Notes_Akshansh

* When n identical stages are cascaded, the gain will rise whereas BANDPASS $(f_H - f_L)$ will decrease.

The product of gain & bandwidth is ALWAYS const.

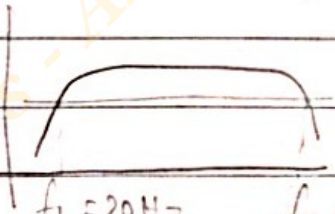
for individual amps (non interacting)



Bandwidth ≃ 39 kHz

Gain as we took = 10

for combined amps



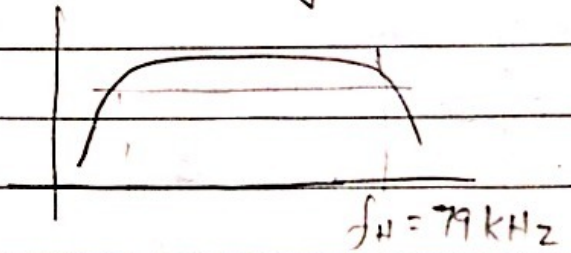
Bandwidth ≃ 20 KHz

Gain, as we want = 1000

(using fig A)

Note :- If stages are INTERACTING, individual stages requires more bandwidth.

for individual stage (interacting)



Bandwidth ≃ 79 KHz

Gain = 10

* Amplifier tuning

→ use of LC circuits (using concept of resonance frequency)

- one LC ckt at i/p
- other LC ckt at o/p.

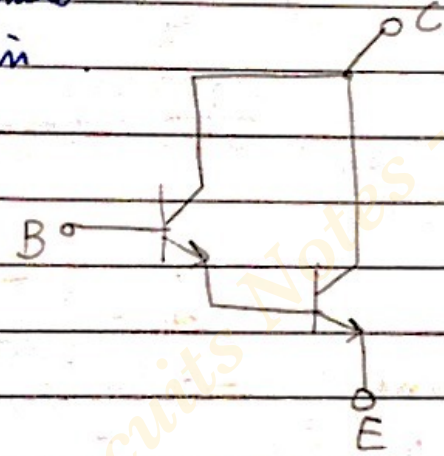
→ Tune one, other gets detuned

Microelectronic Circuits Notes - Akshansh

Note :- :- COMPOSITE PAIRS / COMPOUND DEVICES:

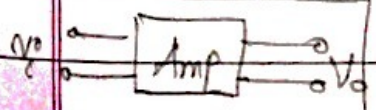
✓ DARLINGTON PAIR:

- an example of Darlington Pair is when emitter of Q1 is tied to base of Q2. & both C's are are tied.
- → 3 terminals.
- → High R_{in}.



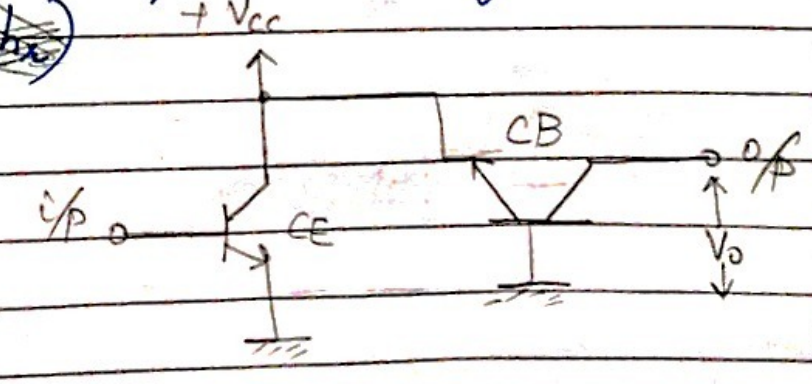
✓ CASCODE PAIR.

- → ∃ ~~CB~~ CE-CB pair
- → extremely small h_r
- → simplified tuning
- → reduces chances of oscill^{n}. Thus, improves stability.



* $\frac{V_o}{V_i}$ = forward gain.

* $\frac{V_i}{V_o}$ = reverse gain ~~(h_r)~~



h_r: a parameter which signifies what is the reverse transfer ratio of a signal.

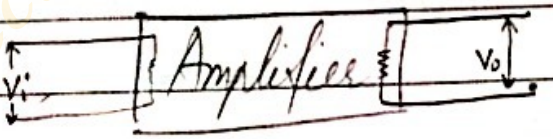
✓ TOTEMPOLE CONFIGUR^{n}.

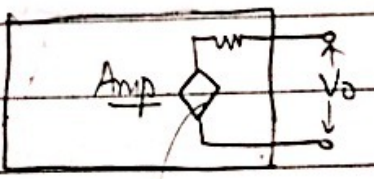
↳ a transistor on another like in "an active load".
→ reduced delay in gates — as against resistive loads due to reduced capacitive loads.
→ Typically also in driver stages.

* Working further on figure A:

Individual	Overall
$R_{i_1}, R_{i_2}, R_{i_3}$	$R_{in_{overall}}$
$R_{o_1}, R_{o_2}, R_{o_3}$	$R_{out_{overall}}$

↳ Now, find Rel^{n} b/w R_i & R_{in}
R_o & R_{out}

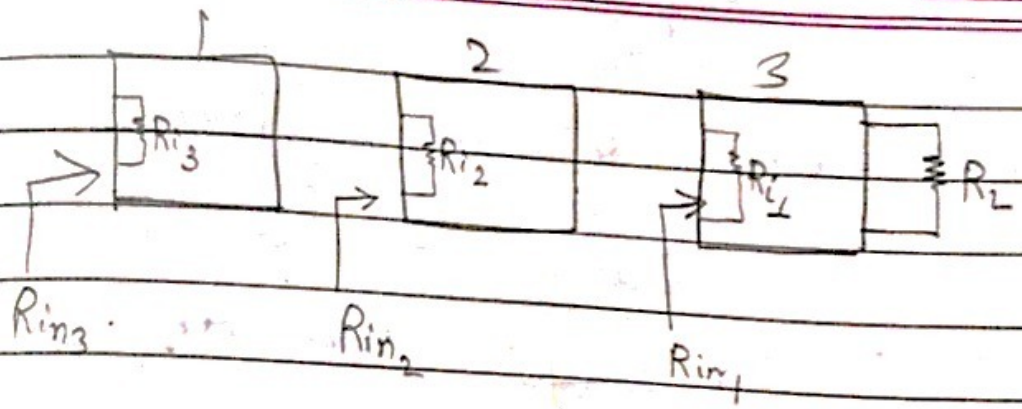




→ $A_{V_0} V_i$

↳ Amplifier's model parameter.

Microelectronic Circuits Notes Akshaya



✓ R_{in_1} is being influenced by loading effect of R_L & R_{i_1}

✓ R_{in_2} is influenced by loading effect of R_{i_1}, R_L → amp 3 & R_{i_2}

✓ R_{in_3} is influenced by loading effect of amp_2 & amp_3 resistors

Basically, the 3 systems are cascaded & rel^n b/w overall & individual depends on the way loading is done at each stage. ☆☆

(Quiz question)

Open book ques. continued

NMos is biased to have $g_m = 1\,mA/V$, $r_o = 100\,k\Omega$; $C_{gs} = 1\,pF$ & $C_{gd} = 0.2\,pF$.

If Find $A_M, f_{P1}, f_{P2}, f_{P3}, f_L, f_H$.

3 IDENTICAL Stage MOSFET Amp → n-channel depletion mosfet

Stage 3

n-channel enhancement

Stage 2

p-channel

n channel

Stage 1

: DISCRETE CKT

FIGURE (A.A)

Microelectronic Circuits Notes by Ishansh

Puffin
Date
Page

Formulae :-

☆ Finding only for stage 1

☆ $A_M = -\frac{R_G}{R_G + R_{sig}} \cdot g_m (R_D \| R_L)$

↳ $R_G = 10 \| 47 = 8.25\ M\Omega$.

$$= -\left[\frac{8.25 \times 10^6}{(8.25 \times 10^6) + (100 \times 10^3)}\right] \times (10^{-3}) \left[4.7K \| 10K\right]$$

$A_M = -3.16$

☆ $f_{p1 \text{ or } p2 \text{ or } p3} = \frac{1}{2\pi C_{ex}(R_G + R_{sig})}$.

↳ $C_{ex} = C_{C1} / C_S / C_{C2}$.

(for f_{P1} for f_{P2} for f_{P3})

☆ $f_H = \frac{1}{2\pi C_{in} R'_{sig}}$

↳ $R'_{sig} = R_{sig} \| R_G$.

☆ $C_{in} = C_{gs} + C_{gd}[1 + g_m(r_o \| R_D \| R_L)]$

☆ $\omega_{P2} = \frac{g_m}{C_S}$

☆ $\omega_{P3} = \frac{1}{C_{C2}(R_D + R_L)}$.

Microelectronic Circuits Notes - Akshansh

★ Model of an FET

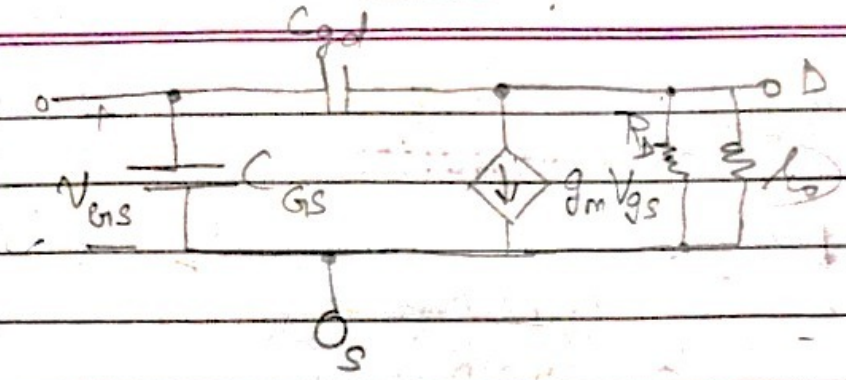
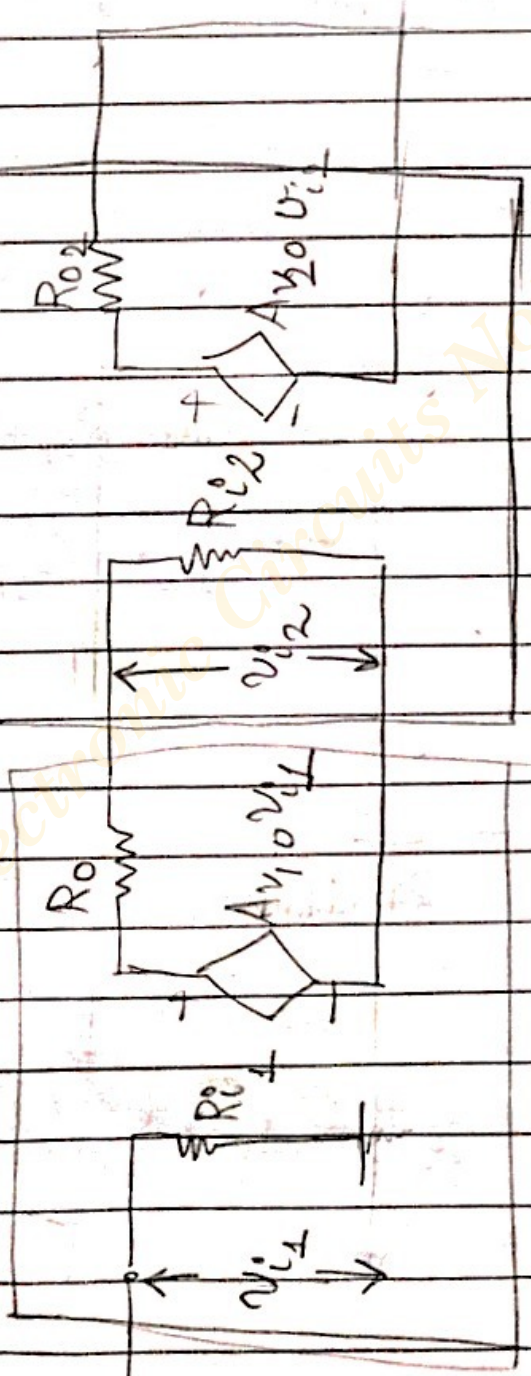


figure (CC)

FIGURE (BB)

Putting circuit model & analysing



★ Figure (AA) : R_1 & R_2 & R_s in each stage are used for biasing.

Microelectronic Circuits Notes - Akshansh

Case ① : Finding Parameters

Considering only stage 1 (fig. AA)

* $f_{P1} = \frac{1}{2\pi C_{C1}(R_G + R_{sig})}$

$\Rightarrow f_{P1} = \frac{1}{2\pi (0.01\mu F)[(8.25\times10^6) + (100\times10^3)]}$

$\Rightarrow f_{P1} = 1.9\ Hz$

Now, * $\omega_{P2} = \frac{g_m}{C_s} = \frac{1\times10^{-3}}{10\times10^{-6}}$

$\omega_{P2} = 10^2\ rad/s$

$f_{P2} = \frac{\omega_{P2}}{2\pi} = \frac{10^2}{2\pi} = 15.92\ Hz$

*

$\omega_{P3} = \frac{1}{C_{C2}(R_D + R_L)} = \frac{1}{10^{-7}(4.7\times10^3 + 10\times10^3)}$

$f_{P3} = \frac{\omega_{P3}}{2\pi} = 108.32$

* $f_H = \frac{1}{2\pi C_{in} \times R_{sig}'}$

$C_{in} = 10^{-12} + (0.2\times10^{-12})\left[1 + 10^3\left(\frac{100\times10^3 // 4.7K //}{100K}\right)\right]$

$100k // 4.7K // 100K$

$= 50K // 4.7K$

$= 4.29K$

$C_{in} = 1.8191 \times10^{-12}\ F$

Microelectronic Circuits Notes - Akshansh

$R_{sig}' = R_{sig} // R_G$

$= (100\,K) // (8.25\,M)$

$R_{sig}' = 0.0988\,M\Omega$

$\therefore f_H = \frac{1}{2\pi (0.0988\,M)(1.819\,p)}$

$\Rightarrow f_H = 891\,kHz$

Case 2: Considering all 3 stages

↓

figure AA

$R_i = R_{G1} // (\infty)$ → Gate to source

$= 8.25\,M\Omega$

↓ Very high

It is what we req^d.

∴ it allows complete V_{sig} to appear as V_{i1}

$R_o = R_{D3} // r_{os}$

R_{D3} = 4.7 K, r_{os} = 100 K → See fig. (cc). The equivalent ckt is shown.

$\Rightarrow R_o = 4.4\,k\Omega$ → very high

Microelectronic Circuits Notes - Akshansh

* VVR: Voltage variable resistance

Puffin
Date
Page

From the open book ques., we needed

$R_i = 1\,M\Omega$. (we got $> 1\,M\Omega$ fine ✓

$R_o = 50\,\Omega$. (we got → $4.4\,K\Omega$ $> 50\,\Omega$ not fine ✗

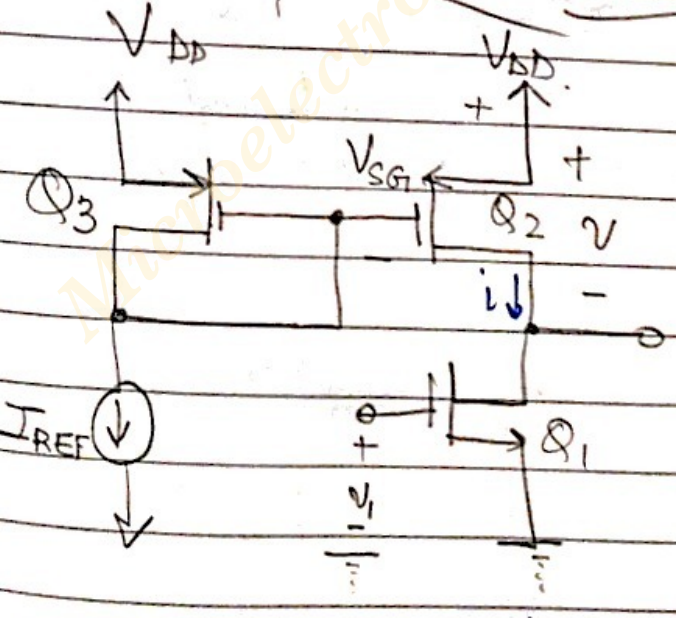
So, put a resistance in ⊥ at o/p as shown by extra R_2 in fig.(AA)

So now, $(R_o) \,//\, 50\,\Omega \cong (49\,\Omega)$

R_o ↓ $4.4K$

$49\,\Omega$ ↓ now this works.

Ily, had we got a lesser value of R_o, put a resistor in series to match up.



✓ IC BIASING Scheme (req'd when implement" done on IC chip)

✓ An alternative circuit of stage 1 of fig(AA) where biasing has been done using current mirror instead of R_1, R_2 & R_S.

✓ This ckt has a stable current source (I_{REF}). So, ✓

Microelectronic Circuits Notes Akshansha

Puffin
Date
Page

Self

example 8.3

* Analysing a ckt differently : ~~ss~~
2 stage CMOS op-Amp config
↳ fig 8.40, 8.41

→ Voltage gain; $A_1 = -g_{m1}(r_{o2} \| R_{o4})$

$A_2 = -g_{m6}(r_{o6} \| R_{o7})$

Other topics for self study :
example 8.4, 8.5

* In any configuration given to us. → like in Ques(AA) before
(Just like in the OPEN book ;)

Options for making a config →

Depletion ✓ BJT
Enhancement ✓ JFET → n channel / p-channel.
Depletion ✓ MOSFET → n channel / p-channel.
Enhancement

for Ques(AA) → open book ques,

BJT ruled out, shown before
So, go to FET.

Microelectronic Circuits Notes - Akshaysh

* Using BJT	Using JFET	Using MOSFET
Rejected	High power consumption	low power consumption

Using Idea (3) :- i.e, using a 2 stage amp :-
Make it s.t stage 1 has gain of 35
& stage 2 also → 35.
So, basically, cascading the stage 1 of fig(AA) twice to get the req^d ckt
Now, we just need to decide for the values of the parameters s.t we get the decided gain of 35
Now, getting all the parameters in 2 stages is difficult.
So, use 3 stages.

The values in fig(AA) * are giving $A_M = -3.16$ per stage. We need 10 so that $10 \times 10 \times 10 = 1000$ gain.

So, the values req^d :-

$C_{C1} = 0.01\,\mu F$
$R_G = 1\,M\Omega$
$R_S = 147\,\Omega$
$C_S = 100\,\mu F$.
$R_L = 22\,k\Omega$.
$C_{C2} = C_{out} = 1\,\mu F$.
$R_D = 2\,k\Omega$ (not given. It is taken by observ^n to get A_V (or A_M) as 10 (or any other value))
$V_{DD} = 20\,V$

} now, using the formulae written before, find all parameters.

Microelectronic Circuits Notes - Akshaya

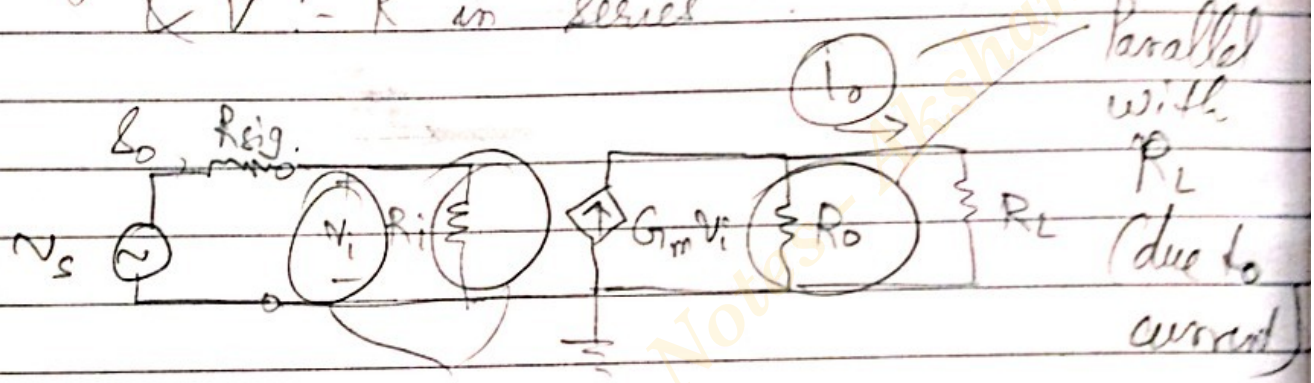
Puffin
Date 14/5/2013
Page 1

✱ Transconductance amplifier

↳ Idea :- Conductance = $\frac{I}{V}$

$\Rightarrow$ I = o/p & V = i/p

for I :- R in parallel
& V :- R in series



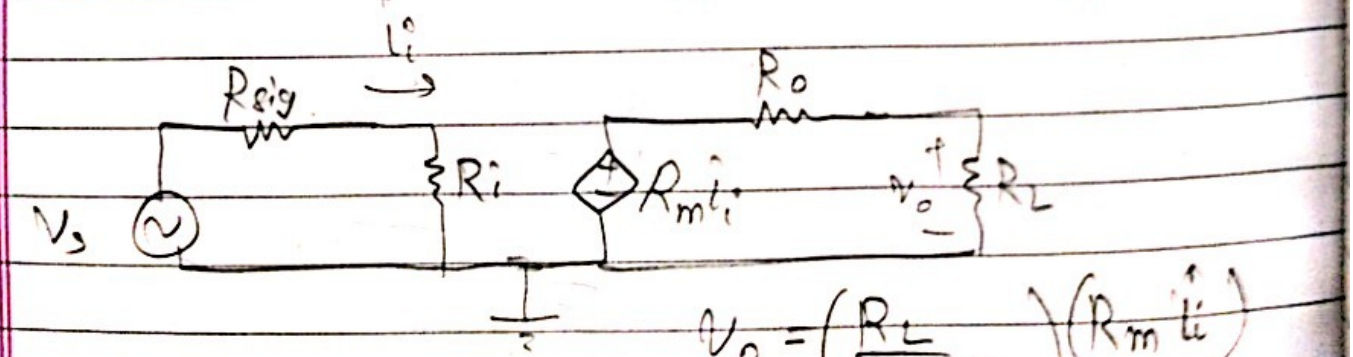
Case

↳ $v_s = v_i \rightarrow R_i >>> R_{sig}$
↳ $i_o = i_L \rightarrow R_o >>> R_L$

✱ Transresistance amplifier

Resistance = $\frac{V}{I}$

$\Rightarrow$ V = o/p & I = i/p

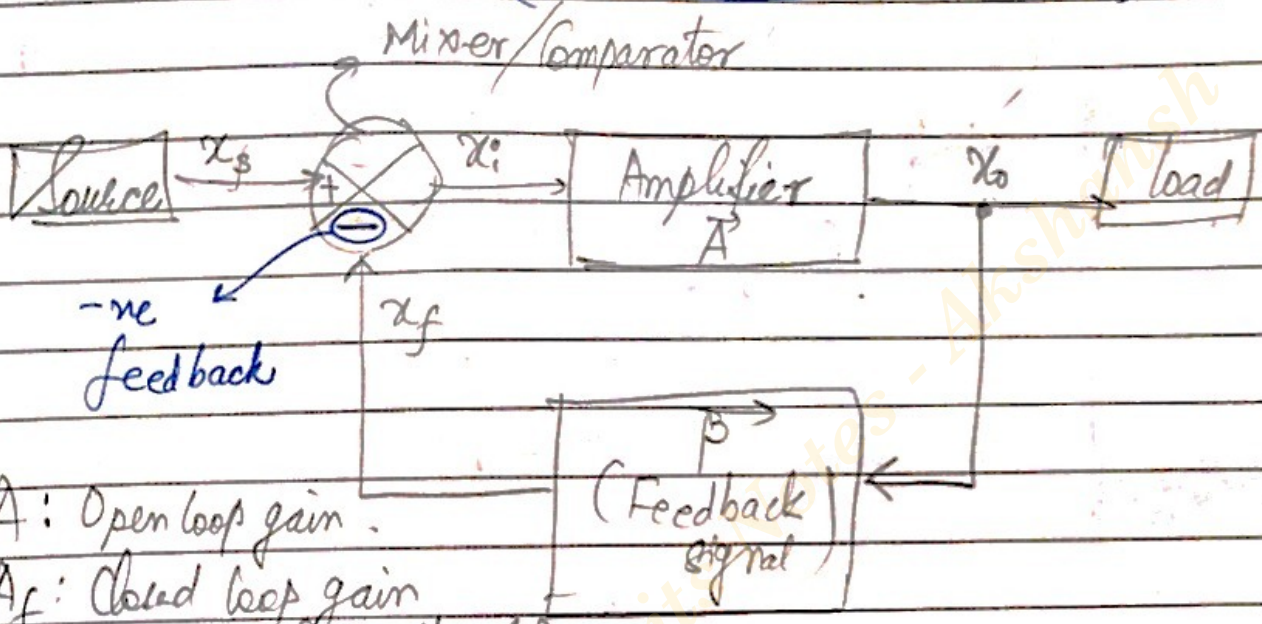


$$v_o = \left(\frac{R_L}{R_L + R_o}\right)\left(R_m i_i\right)$$

Microelectronic Circuits Notes - Yashansh

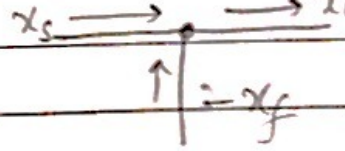
A : Amplifier's gain, taking loading of f/b amp into account, but, without feedback

Ch - FEEDBACK AMPLIFIER



A : Open loop gain.
A_f : Closed loop gain (with feedback)

① $x_s - x_f = x_i$ (See the comparator as a node →



By KCL, $x_s + (-x_f) = x_i$

★ $\beta = \frac{x_f}{x_o}$

② $A = \frac{x_o}{x_i}$

③ $A_f = \frac{x_o}{x_s} = \frac{A x_i}{x_s} = \frac{A x_i}{x_i + x_f} = \frac{A x_i}{x_i + \beta x_o}$

$\Rightarrow A_f = \frac{A x_i}{x_i + \beta(A x_i)} = \frac{A}{1 + \beta A}$

$\Rightarrow$ ★ $\boxed{A_f = \frac{A}{1 + \beta A}}$ → β : loop gain

Microelectronic Circuits Notes - Akshmish

Puffin
Date
Page

* for (-ve f/b), βA has to be of opposite sign

$$\left(\therefore A_f = \frac{A}{1+\beta A}\right)$$

So, for that $\frac{x_f}{x_o} \times \frac{x_o}{x_i} > 0$

$$\Rightarrow \frac{x_f}{x_i} > 0$$

So, x_f & x_i should have same sign

If x_f & $x_i > 0$

Then, $x_i = x_f - x_i$

→ Difference signal.

i.e, ($x_i < x_f$, basically)

So, $A_f < A$ & the reduction factor is $(1+\beta A)$

$1+\beta A$: called as DE-SENSITIVITY FACTOR

More the f/b, more is reduction on A

If $\beta A >> 1$

$$\hookrightarrow A_f = \frac{A}{\beta A} = \frac{1}{\beta}$$

So, with very high values of Aβ, A_f becomes independent of A (or) Closed loop gain becomes less dependent on Openloop gain of amp.

Microelectronic Circuit Notes - Akshansh

Puffin
Date
Page

★ This property is desirable

↳ We want closed loop gain to be const (accurate)

Usually, A (open loop gain) depends on a lot of parameters

the parameters can be temperature of junction, of sys.

If this changes, A_f will also change ($\because A_f = \frac{A}{1+\beta A}$)

So, in -ve f/b, $A_f = \left.\frac{1}{\beta}\right|_{\beta A >> 1}$

So, it becomes independent of A, & hence, sort of const!

★ $A_f = \frac{A}{1+A\beta}$.

$\Rightarrow \left(\frac{x_o}{x_s}\right) = \left(\frac{A}{1+A\beta}\right)$

$\Rightarrow x_o = \left(\frac{A}{1+A\beta}\right) x_s$

$\Rightarrow \frac{x_f}{\beta} = \left(\frac{A}{1+A\beta}\right) x_s$

$\Rightarrow x_f = \left(\frac{A\beta}{1+A\beta}\right) x_s$

So, for $A\beta >> 1$

$x_f = x_s$

$\Rightarrow$ Source signal = f/b signal

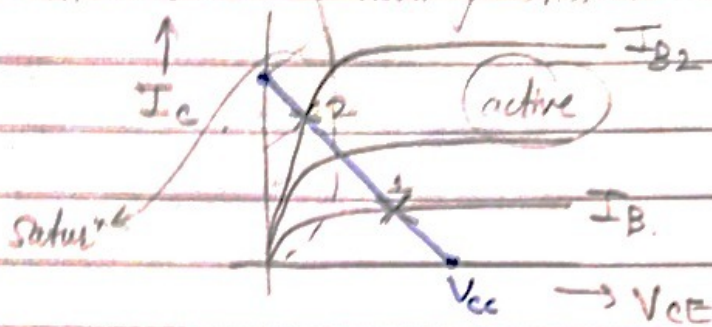
So, difference signal $\longrightarrow 0$.

Microelectronic Circuits Notes Akshansh

The gain depends on temperature.

how?

↳ any amplifier / physical ckt → made of semiconductor having characteristics



$T \uparrow$, $I_B \uparrow$. So, $I_{B1} \rightarrow I_{B2}$

Pt (1) → Bias Point changes to Pt (2).

So, from active region → amplifier changes to satur" region.

So, amplifier won't work

So, we don't want A_f to depend on A

So, -ve f/b is preferred.

The total gain is lesser than A

($A_f < A$: for -ve f/b)

But at the same time, we are getting a const value → STABILITY.

(We have to compensate for 1 thing to get the other).

☆ Properties of -ve f/b

- Gain De-sensitivity
- Bandwidth extension → Gain × Bandwidth = const. Gain ↓, so, Bandwidth ↑
- Red" in Non linear Distortion.
- Substantial red" in frequency distortion.

The linear curve theory

Microelectronic Circuits Notes Akshansh

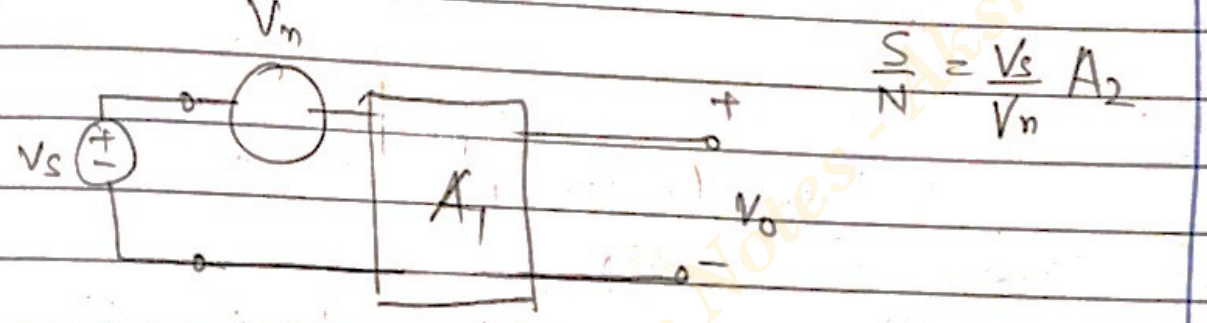
linear curve theory

- Red^n in noise
- Improved Terminal Characteristics : R_i & R_o → values of

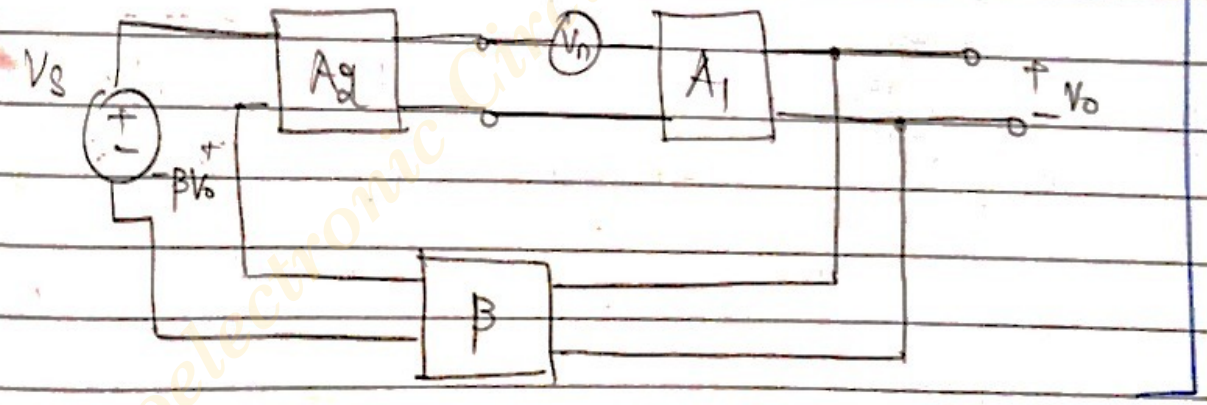
→ DETAIL

* $V_o = V_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta}$

fig 8.2 *



$\frac{S}{N} = \frac{V_s}{V_n} A_2$



* 4 basic topologies exist for -ve f/b amps.

fig 8.4 #

- for voltage amp.
- for current amp
- for transresistance amp
- for current amp.

for current
Series : sampling
Parallel : mixing → KCL

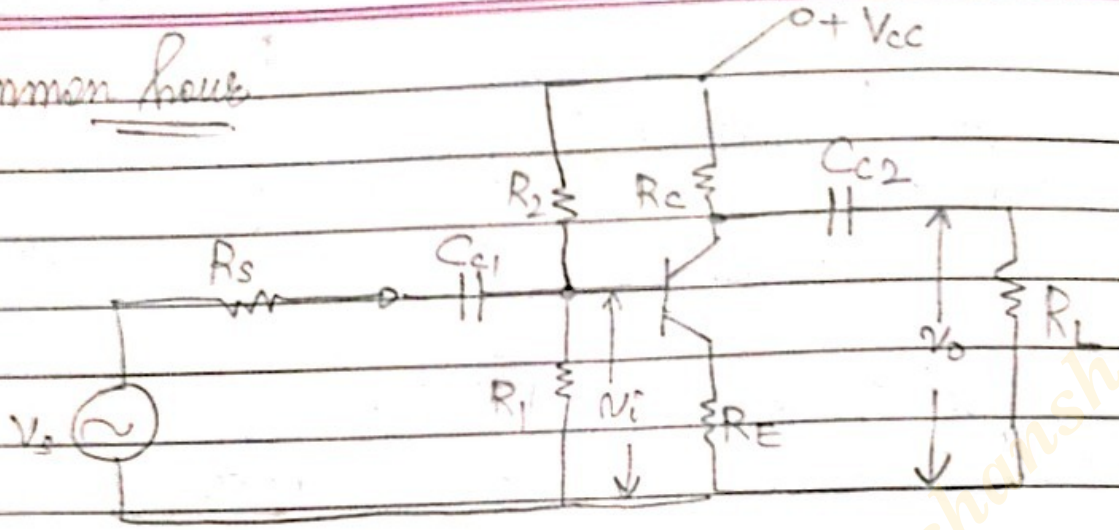
for voltage
Series : mixing → KVL
Parallel : sampling

Microelectronic Circuits Notes_Akshansh

Puffin
Date 16/5/13
Page

Common base

Q

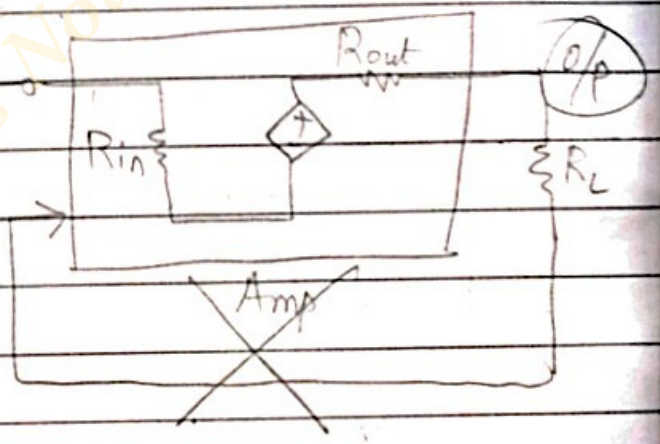


Identify the feedback, if one exists.

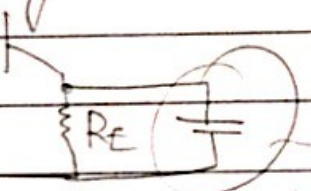
WRONG IDEA

$R_{in} = (R_1 \parallel R_2) \parallel R_E$

$R_{out} = R_C$



For the circuit given, ∃ no capacitance with R_E i.e

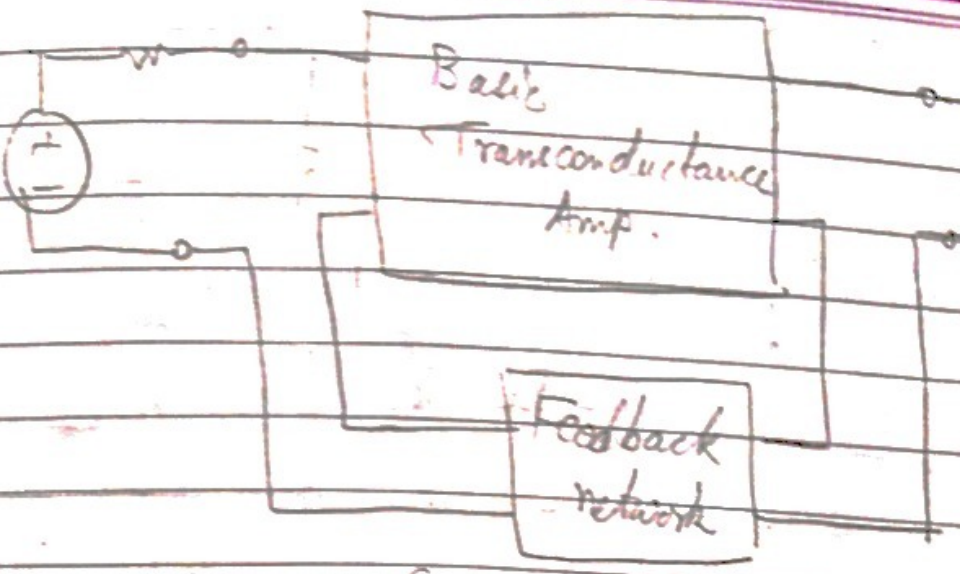


So, when seeing the AC only, the Resistance won't vanish (∵ C isn't there)

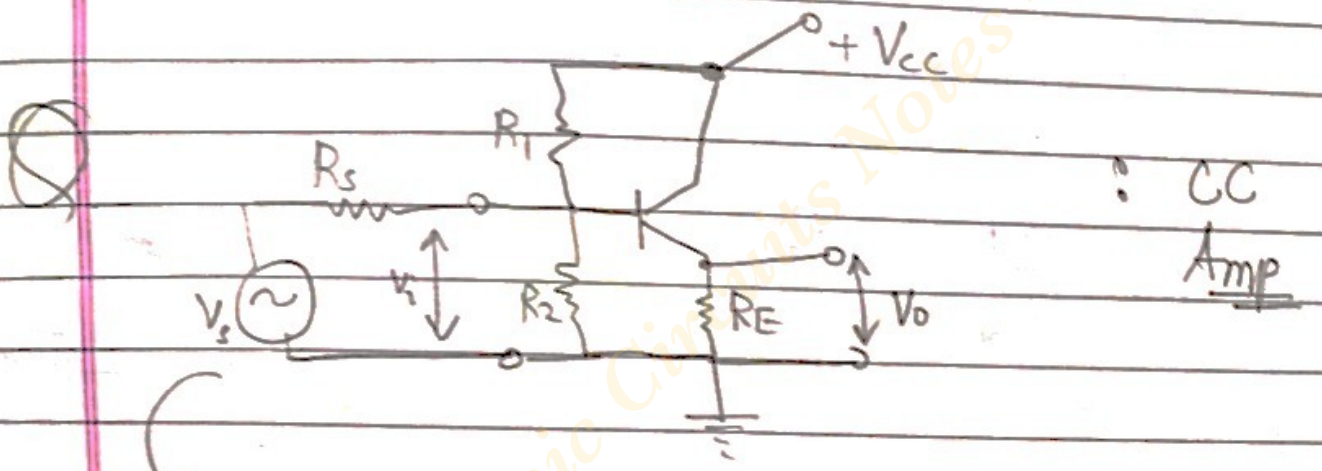
So, R_E is a common pt. b/w i/p & o/p.

The ckt can be seen sth like →

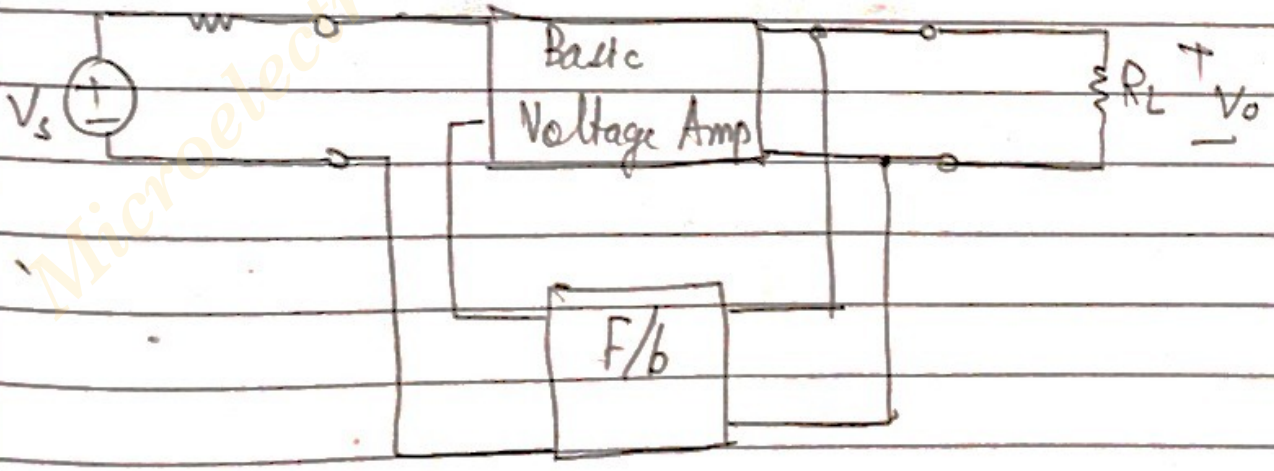
Microelectronic Circuits Notes - Akshansh



Series - series



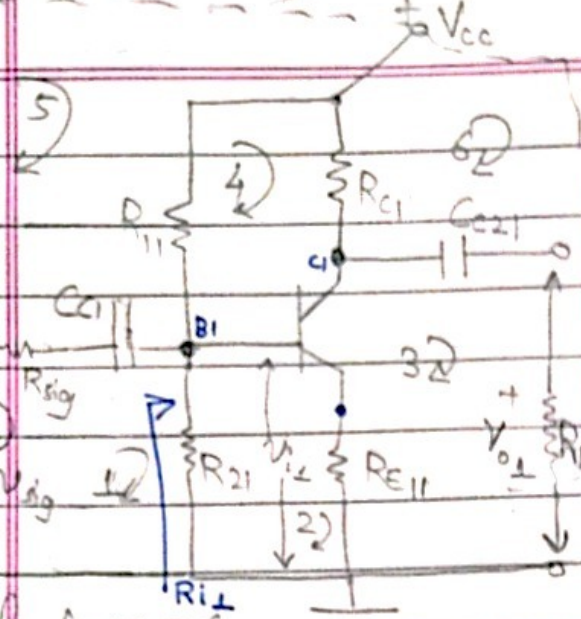
: CC Amp



Series - shunt topology

Microelectronic Circuits Notes - Akshansh

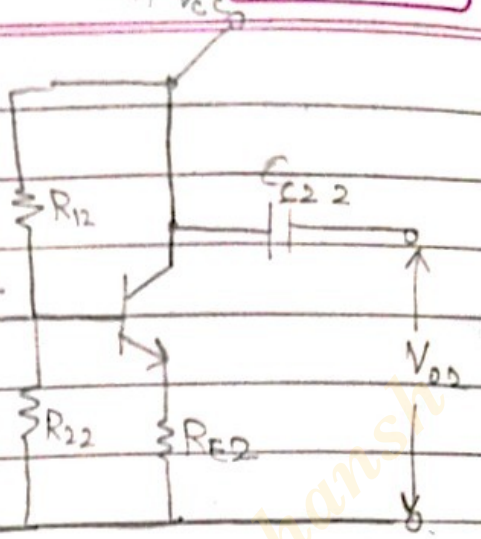
(fig. M)



no. of loops = 6

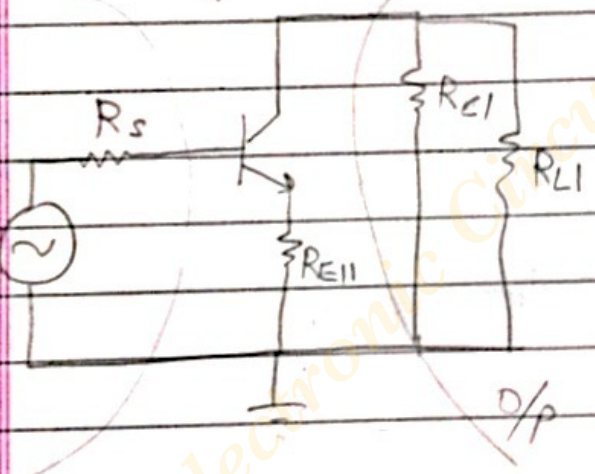
Series-Series topology

(fig N)

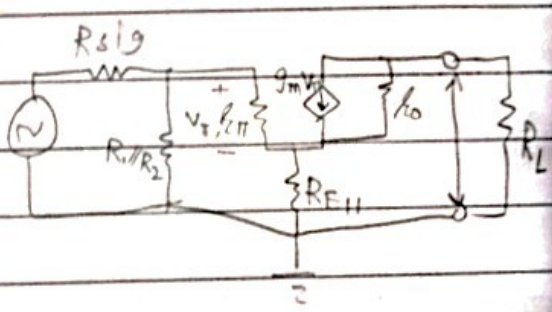


Series-shunt topology

AC equivalent



≡



using hybrid-π model

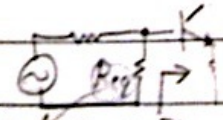
Q:- Why R_1 & R_2 are not present?

Ans:- 1) Its an AC equivalent ckt

2) In AC equivalent ckt, bias components are not shown by convention

R_1 & R_2 participate in biasing.

In practice,

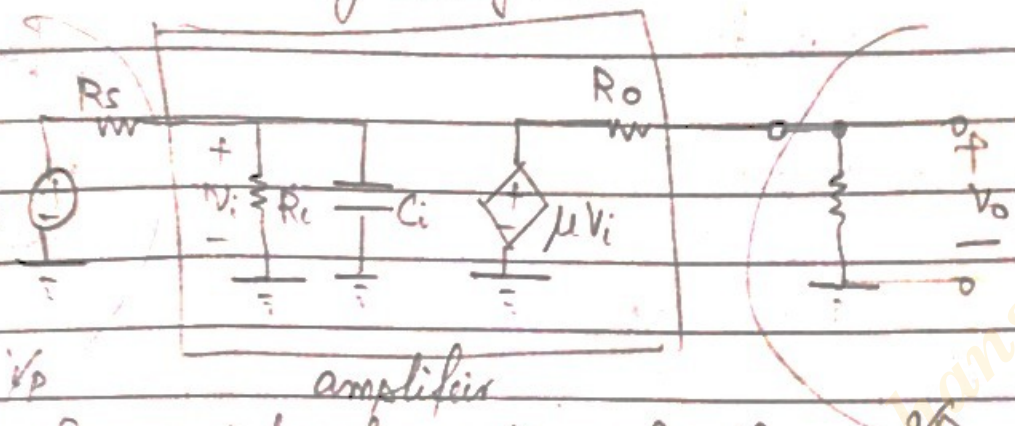


$R_1 // R_2 \gg R_{in}$

Microelectronic Circuits Notes - Akshansh

MY CONCEPTS

Note :- Consider the following ckt :-



The C_i shown : internal capacitance for the amp.
As visible from fig, it is a voltage amplifier, i.e, the dependent voltage source is depending on the value of i/p voltage V_i. (μV_i)

Remember :- Capacitance will eat up any voltage that is developed across it & that voltage won't contribute to amplific^n. So, higher the voltage across C_i, lower is amplific^n.

Now, Impedance across C_i is given as $X_c = \frac{1}{j\omega C_i}$

At small value of ω (frequency), X_c becomes large. So, voltage across C_i becomes large (not desirable).

Hence, for low frequency i/p, the effect of capacitance is ignored (by assuming $C_i \to \infty$ s.t $1/j\omega C_i$ is small only).

At high value of ω, X_c becomes small. So, high voltage drop across C_i i.e, C_i eats less of i/p voltage. Hence, the effect of internal capacitances is taken into account for higher frequencies.

Microelectronic Circuits Notes- Abhishek

Analysis : with & without f/b

Using fig for M's → equivalent

without f/b (CE Amp)	with f/b (CE with Emitter Resis.)
✱ $R_{in} = R_B // r_\pi$	✱ $R_{in} = R_B // (1+\beta)(r_e + R_e)$
For $R_B >> r_\pi$	Now $r_\pi = (1+\beta) r_e$
$R_{in} = r_\pi$.	For R_B v.v. high,
	$R_{in} = (1+\beta)(r_e + R_e)$
	$= r_\pi + (1+\beta) R_e$
	∴ with f/b, R_{in} is high (as desired)
✱ $R_{out} = r_o // R_C$	✱ $R_{out} = R_C$
r_o is very high	
For RB $r_o \to \infty$	
∴ $R_{out} \simeq R_C$	
∴ no change in R_{out}	
✱ $A_v = -g_m (r_o // R_C // R_L)$	✱ $A_v = \frac{-\alpha (R_C // R_L)}{r_e + R_E} \simeq \frac{-g_m (R_C // R_L)}{1 + g_m R_E}$
$r_o \to \infty$.	
∴ $\infty // (\ ) = (\ )$	
∴ $A_v \simeq -g_m (R_C // R_L)$	
∴ Voltage gain decreases with f/b.	

Microelectronic Circuits Notes - Akshansh

(Book) → Q. 3.24 (B.U. 2.5)

Using CC Amp (Voltage Amp.)

$$R_{out} = R_o \parallel \left[r_e + \frac{R_{sig} \parallel R_B}{1+\beta} \right]$$

Assuming $R_B \to \infty$

$R_{sig} \to$ small

$1+\beta \to$ high $\Rightarrow \frac{R_{sig}}{1+\beta} \to 0$

$R_o \to$ high

$R_o, R_o \parallel r_e \simeq r_e$

$r_e \cdot R_{sig}$

$\therefore R_{out} = R_{sig}$, as reqd

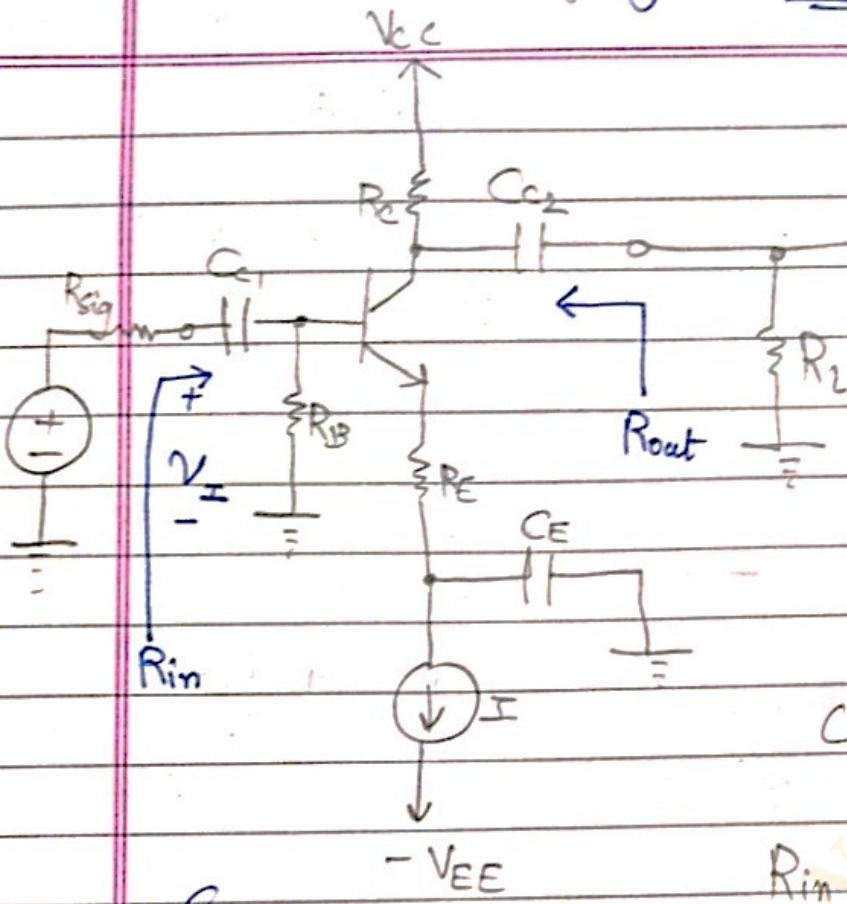
$$R_{in} = R_B \parallel (1+\beta)[r_e + (R_o \parallel R_L)]$$

By same above direct analysis,

$R_{in} \to$ very high, as reqd for voltage amp.

Microelectronic Circuits Notes - Akshansh

CE Amp R_E un-by-passed. Current Series feedback.



Series-series f/b

* Obtain A_V & R_{in} of a CE Amp circuit if R_E is not by-passed.

CE Amp. with R_E

$$R_{in} = R_B \,//\, (1+\beta)(r_e + R_E)$$

$$A_V = \frac{-\alpha (R_C \,//\, R_L)}{r_e + R_E}$$

$$\cong \frac{-g_m (R_C \,//\, R_L)}{1 + g_m R_E}$$

CE Amp

$$R_{in} = R_B \,//\, r_\pi = R_B \,//\, (1+\beta) r_e$$

$$A_V = -g_m (r_o \,//\, R_C \,//\, R_L)$$

$$\frac{V_o}{V_i} = -\frac{h_{fe}}{h_{ie}} R_C \quad \text{(with } C_E\text{)}$$

$$\frac{V_o}{V_i} = -\frac{R_C}{R_E} \quad \text{(with } C_E\text{)}$$

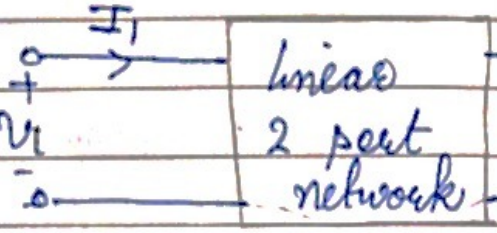
Microelectronic Circuit Notes Akshansh

APPENDIX-B

$I_1, I_2 =$

Puffin
Date
Page

★ Two Port Network: $f(V_1, V_2)$ Eqns :-



$$I_1 = y_{11}V_1 + y_{12}V_2$$
$$I_2 = y_{21}V_1 + y_{22}V_2$$

$$V_1 = z_{11}I_1 + z_{12}I_2$$
$$V_2 = z_{21}I_1 + z_{22}I_2$$

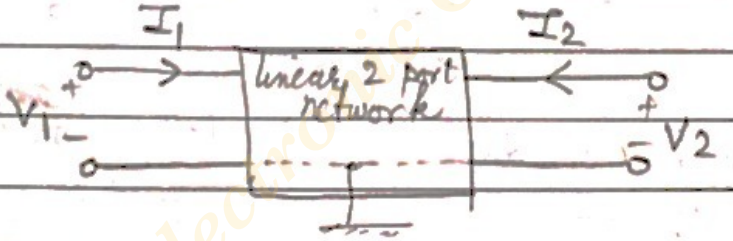
$V_1, V_2 = f(I_1, I_2)$

- Set of 2 terminals at i/p is called : i/p port
  o/p is called : o/p port

$$V_1 = h_{11}I_1 + h_{12}V_2$$
$$I_2 = h_{21}I_1 + h_{22}V_2$$

$V_1, I_2 = f(I_1, V_2)$

- Amplifier modelled as a 2 port network is shown below.



The above eqns are for this network.

Definitions :- → we are giving a defn.

Y-parameter Model (a)

$$y_{11} \triangleq \left.\frac{I_1}{V_1}\right|_{V_2=0} \qquad y_{12} \triangleq \left.\frac{I_1}{V_2}\right|_{V_1=0}$$

$$y_{21} \triangleq \left.\frac{I_2}{V_1}\right|_{V_2=0} \qquad y_{22} \triangleq \left.\frac{I_2}{V_2}\right|_{V_1=0}$$

Z-parameter Model (b)

$$z_{11} \triangleq \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad z_{12} \triangleq \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

$$z_{21} \triangleq \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad z_{22} \triangleq \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

not used for BJT/FET AMPLIFIERS

Microelectronic Circuits Notes - Akshansh

→ hybrid

h-parameter Model (c)

i/p resistance = h_i

reverse voltage gain = h_r

$h_{11} \triangleq \left.\frac{V_1}{I_1}\right|_{V_2=0}$ $\quad h_{12} \triangleq \left.\frac{V_1}{V_2}\right|_{I_1=0}$

$h_{21} \triangleq \left.\frac{I_2}{I_1}\right|_{V_2=0}$ $\quad h_{22} \triangleq \left.\frac{I_2}{V_2}\right|_{I_1=0}$

forward current gain = h_f

o/p admittance = h_o

More suited for Amp modelling (∵ all terminal char. can easily be got)

✱ Different type of models (device ckt)

~~High~~ low frequency : hybrid π : VCCS, CCCS.
T- model : VCCS, CCCS

High frequency : hybrid - π.

5 models.

5 for BJT

5 for FET.

10 ~~total models~~.

5 for CB Amp
5 for CE
5 for CC.

→ 15 models

5 for CS Amp
5 for CD
5 for CG

→ 15 models

✱ ∃ 3 more models :- h-parameter
Z- "
Y- "

} 3

Microelectronic Circuits Notes - Akshansh

☆ Consider an h-parameter model

Its model parameters are : h_i, h_f, h_r, h_o

For CE Amp :- h_{ie}, h_{fe}, h_{re}, h_{oe}

CC Amp :- h_{ic}, h_{fc}, h_{rc}, h_{oc}

CB Amp :- h_{ib}, h_{fb}, h_{rb}, h_{ob}

Ily for CS, CD & CG Amp

Microelectronic Circuits Notes - Akshansh

§ The Series-Series f/b amplifier

A-CIRCUIT

↳ The equivalent ckt of the amp without f/b, but, taking into account loading of the f/b network on the amplifier's i/p or o/p sides.

Imp Self fig 7.16, 7.11, 7.20, 7.24

Imp 4. TOPIC: o/p STAGES & POWER AMPLIFIERS

Microelectronic Circuits Notes - Akshanth

✱ CLASS-A Power Amp

✱ Max. signal waveforms & Theoretical max. efficiency.

All formulas relating to fig 14.4

Power conversion efficiency

$\eta = \frac{\text{load power } (P_L)}{\text{Supply power } (P_S)}$

The avg. load power will be

$P_L = \frac{(V_{o\text{-peak}}/\sqrt{2})^2}{R_L} = \frac{1}{2}\frac{V_{o\text{-peak}}^2}{R_L}$ ($\because$ Sinusoidal)

rms value of AC sine wave

Power drawn from +ve supply is $V_{cc}I$.

$P_S = 2V_{cc}I$ ($\because$ that of +ve supply too)

$\therefore \eta = \frac{1}{4}\frac{V_{o\text{-peak}}^2}{IR_L V_{cc}} = \frac{1}{4}\left(\frac{V_{o\text{-peak}}}{IR_L}\right)\frac{V_{o\text{-peak}}}{V_{cc}}$

Since $V_{o\text{-peak}} \leq V_{cc}$ & $V_{o\text{-peak}} \leq IR_L$:

Max efficiency is obtained when

$V_{o\text{-peak}} = V_{cc} = IR_L$

$\Rightarrow$ attainable theoretical maximum is

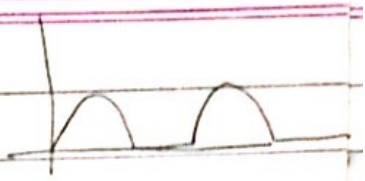
$\eta_{max} = 25\%$.

✱ SLEW RISE: Rate of rise of o/p for given rate of rise in i/p

Microelectronic Circuits Notes - Akshansh

✱ CLASS-B

✱ Cross band over distortion.
(due to dead band)
(fig 14.7, 14.8)



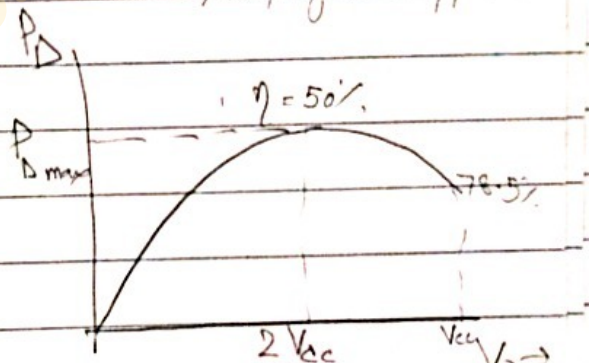
✱ $\eta = 50\%$ at the pt. of $P_{D\,max}$

$$\eta = \frac{1}{2}\left(\frac{V_{o\text{-}peak}^2}{R_L}\right) \div \left(\frac{2V_{o\text{-}peak}}{\pi \times R_L} V_{cc}\right)$$

$$= \frac{\pi}{4}\frac{V_{o\,peak}}{R_L} \Rightarrow \eta_{max} = \underline{78.5\%}.$$

Amplifier happened

$$P_{D\text{-}max} = \frac{2}{\pi^2}\frac{V_{cc}^2}{R_L}$$



(fig 14.8)

✱ Reducing crossover distortion in class B
(fig 14.9)
↳ Using op-amp in f/b.
↳ Dead band reduces to ± 0.7 V/A. Volts.

Electronic Circuits Notes - Arshansh